Problem #1 – Self-loaded NAND Delay

a) Use HSPICE to find the average propagation delay for a NAND gate in this process for a fanout of 1, 2, 3, and 4. Plot the propagation delay as a function of the fanout.

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* ee141 hw5: 4-stage nand chain

.param clload="20f"
.param fanout="4"

.lib '/home/ff/ee141/MODELS/g25.mod' TT

* nand

.subckt nand in1 in2 out vdd gnd
m1 out in2 x gnd nmos w=2u l=.25u
m2 x in1 gnd gnd nmos w=2u l=.25u
m3 out in1 vdd vdd pmos w=2u l=.25u
m4 out in2 vdd vdd pmos w=2u l=.25u
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* nand plus capacitive load at output

.subckt nandcap in vdd gnd
x1 vdd in out vdd gnd nand
c1 out 0 'cload'
.ends

* load nand plus fanout

.subckt nandload in vdd gnd
x1 vdd in out1 vdd gnd nand
x2 out1 vdd gnd nandcap m='fanout'
.ends

* main deck

* 4-stage nand chain
x1 vdd stepin in vdd 0 nand
x2 vdd in out vdd 0 nand
x3 vdd out out2 vdd 0 nand
x4 out2 vdd 0 nandcap m='fanout'

* loading nand's
x2load in vdd 0 nandload m='fanout-1'
x3load out vdd 0 nandload m='fanout-1'

* voltage sources
vdd vdd 0 dc 2.5
vin stepin 0 pulse (0 2.5 100p 200p 200p 800p 10n)

.tran 1p 2n
.measure tplh trig V(in) val=1.25 fall=1 targ v(out) val=1.25 rise=1
.measure tphl trig V(in) val=1.25 rise=1 targ v(out) val=1.25 fall=1

.end
b) What is the self-loaded delay of a NAND gate?

Self-loaded delay = 44.0ps

c) What is the slope of the best-fit line through your data points (additional delay per fanout)? This slope is related to the number obtained from logical effort calculations when you divide by the slope for an inverter (HW5 problem 4)…compare slope_{NAND}/slope_{INV} to the theoretical value from logical effort.

Slope = 25.8ps per fanout

Slope ratio = 25.8 / 21.2 = 1.22

This is close to the logical effort value of 1.33.

d) From your answers to b) and c), find the C_d/C_g. Compute C_g and C_d.

\[
C_d/C_g = \text{Self-loaded delay} / (\text{Delay for one fanout} – \text{Self-loaded delay})= 44.0 / 25.8 = 1.71
\]

\[
C_g = (3.9 * 8.85e-14 \text{ F/cm} / 58\text{Å}) * (2\mu\text{m} + 2\mu\text{m}) * 0.25\mu\text{m} = 5.95fF
\]

\[
C_d = 1.71 * C_g = 10.17fF
\]

This drain capacitance is bigger than for the inverter…which makes sense because we’re hooking up more devices to the output…and the transistor W’s are bigger as well.
e) Compute $R_{eq}$.

Using the self-loaded delay:

$$R_{eq} = \frac{t_{p,\text{self-load}}}{(0.69 \times C_d)} = \frac{44.0 \text{ ps}}{0.69 \times 10.17 \text{fF}} = 6.27 \text{k\Omega}$$

The $R_{eq}$ is similar to the value we found for the inverter, which makes sense because we doubled the W's for the stacked NMOS transistors.

Problem 2

a) Logical effort of a 3-input nand gate=5/3

b)

$B=b_1*b_2*b_3*b_4*b_5*b_6=1*2*3*1*1*1=6$

$F=100\text{fF}/3\text{fF}=100/3$

$G=g_1*g_2*g_3*g_4*g_5*g_6=1*4/3*5/3*1*5/3*4/3=4.9383$

$H=BFG=6*100/3*4.9383=987.6543$

Optimal effort per stage $h = (987.6543)^{1/6}=3.1557$

c)

$f_1=h/g_1=3.1557$

$f_2=h/g_2=2.3668$

$f_3=h/g_3=1.8934$

$f_4=h/g_4=3.1557$

$f_5=h/g_5=1.8934$

$f_6=h/g_6=3.1557$

$X=3fF*f_1/b_1=9.467fF$

$Y=X*f_2/b_2=11.204fF$

$Z=Y*f_3/b_3=7.0711fF$

$W=Z*f_4/b_4=22.314fF$

$V=W*f_5/b_5=42.251fF$

Sanity Check: $V*f_6=CL=100fF$

Problem 3

use 2-input pre-decoder and the diagram is following. And note that the branching factor of NAND is 4.

$F=A0\cdot A1\cdot A2\cdot A3'= (A0+A1)'\cdot (A2+A3)'$
B=4
F=30
G=5/3*4/3=20/9
H=2400/9
h= (2400/9)1/3 = 6.43
f1=h/g1=3.86
f2=h/g2=4.82
f3=h/g3=6.43

No detailed capacitance value is given, so no numerical solution for the sizing.