PROBLEM 1: INVERTER SIZING AND LOADS

In this problem, we will use inverter sizing to minimize the propagation delay required to drive a fixed capacitive load with a fixed input capacitance. Assume that \( V_{DD}=2.5\,V \), \( C_{in}=4.5\,fF \) and \( \gamma=1 \) for all parts of this problem.

a) Determine the optimal number of stages for an inverter chain that is driving a load capacitance 100 times the input capacitance of the first inverter in the chain. Don’t worry about getting the polarity of the signal right (i.e., you can use either an even or an odd number of inverters in your chain).

b) Draw the schematic of the inverter chain and size each inverter. You do not need to draw each transistor – a gate level schematic (with transistor sizes) is sufficient.

c) What is the propagation delay of this circuit? You may leave your answer in terms of \( t_{inv} \). What is the dynamic power consumption of the inverter chain when its input is a clock whose frequency is 200MHz? (Note that you shouldn’t forget to include the power consumed by driving the input capacitance of the first inverter.)

PROBLEM 2: SIDE-LOADS

We have so far ignored any fixed capacitive load between the inverters in an inverter chain, but in a real chip, these devices and gates are connected through metal interconnect. In certain cases, these devices may be placed sufficiently far apart that the delay and power may be affected by the parasitic resistance and capacitance of the wires. For this problem, we will ignore the resistance of the interconnect and only model the capacitive component.

Consider the inverter chain shown above, where \( C_{in} = 4.5\,fF \) and \( C_L = 64C_{in} \). There is a fixed (i.e., independent of sizing) capacitance of \( C_{fixed} = 64C_{in} \) between the second and third inverters in the chain. This fixed capacitance is sometimes called a side-load.
a) Derive the equation for the delay of this inverter chain in terms of the input capacitances of the three inverters (C₁, C₂, C₃), the capacitances C_{fixed} and C_L, γ, and t_{inv}.

b) Using the values for C_{in} and C_L we have provided and your equation from part a), determine the optimal sizing for the inverters to minimize the total delay.

c) We will now explore an alternative heuristic to size the inverter chain. First, pretend that the side-load doesn’t exist, and calculate the optimal size for the last inverter. Leaving the sizing of this last inverter constant and re-introducing the side-load, you can now calculate the total fanout that the first two inverters must drive. Based on this total fanout for the first two inverters, you can now size the second inverter using the standard method we learned in class. Show your work and include a gate-level schematic of the new inverter chain.

d) In terms of t_{inv}, what is the delay of the inverter chain from part b)? How does this compare to the delay of the inverter chains in part c)? You may assume γ=1.

e) What is the dynamic power consumption of the chain from part b)? What about the chain from part c)? What is the ratio of dynamic power consumption between the two chains? You may assume γ=1, V_{DD} = 2.5V, \( \alpha_{0,\gamma} = 0.5 \), and \( f_{clk} = 200\text{MHz} \).

**PROBLEM 3: TECHNOLOGY SCALING**

A recent microprocessor has been designed in a 65nm technology with a standard threshold voltage of 0.3V. The chip runs at 3GHz with a 1.2V power supply and a total power consumption of 100 watts. Out of this 100W of total power, 30W is due to subthreshold leakage in the transistors.

a) Use the full scaling model (and assume velocity saturated devices) to calculate the new clock frequency, supply voltage, and power consumption when the chip is scaled down to a 45nm technology. You should assume that leakage current is modeled using the formula:

\[ I_{\text{leakage}} = W I_0 e^{-\frac{V_T}{1.5 \times 0.025}} \]

where \( I_0 \) is the same in both the 65nm and 45nm technologies. In other words, you can ignore DIBL.

b) Redo the calculations in part a) using the fixed voltage scaling model instead.

c) Let’s now assume that in moving to the 45nm node, instead of increasing the clock frequency, we doubled the number of processor cores, and that each of these cores continues to run at 3GHz. Assuming \( V_T \) remains 0.3V and velocity saturated devices, calculate the minimum supply voltage required for the cores to
operate at 3GHz. With this supply voltage, what would be the power consumption of the new 45nm chip? You may assume that $\xi_{\text{crit}} = 2.52\text{V/µm}$. 