Administrative Stuff
- Project phase 1 due on Thursday
  - Report template posted on the web
- Midterm 2 next Tuesday

Dynamic CMOS
- In static circuits, at every point in time (except when switching) the output is connected to either GND or $V_{DD}$ via a low resistance path.
  - fan-in of $n$ requires $2n$ ($n$ N-type + $n$ P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - only requires $n + 2$ ($n+1$ N-type + 1 P-type) transistors

Class Material
- Last lecture
  - Pass-transistor logic
- Today’s lecture
  - Dynamic logic
- Reading
  - Chapter 6

Dynamic Gate
Two phase operation
- Precharge (CLK = 0)
- Evaluate (CLK = 1)
**Dynamic Gate**

Two phase operation
- **Precharge** (Clk = 0)
- **Evaluate** (Clk = 1)

**Conditions on Output**
- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on $C_L$.

**Properties of Dynamic Gates**
- Logic function is implemented by the PDN only
  - number of transistors is $N + 2$ (versus 2N for static complementary CMOS)
  - Full swing outputs ($V_{OL} = \text{GND}$ and $V_{OH} = V_{DD}$)
  - Non-ratioed - sizing of the devices does not affect the logic levels
  - Faster switching speeds
    - reduced load capacitance due to lower input capacitance ($C_{in}$)
    - reduced load capacitance due to smaller output loading ($C_{out}$)
    - no $I_{sc}$, so all the current provided by PDN goes into discharging $C_L$
- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between $V_{DD}$ and GND (including $P_{on}$)
  - no glitching
  - higher transition probabilities
  - extra load on Clk
  - PDN starts to work as soon as the input signals exceed $V_{TN}$, so $V_M$, $V_{IH}$, and $V_{IL}$ equal to $V_{TN}$
  - low noise margin (NML)
- Needs a precharge/evaluate clock

**LE of Dynamic Gates**

**Issues in Dynamic Design 1: Charge Leakage**

Dominant component is subthreshold current
Solution to Charge Leakage

Same approach as level restorer for pass-transistor logic.

Dynamic Gate VTC

\[ V_{\text{out}} = \begin{cases} V_N & \text{if } V_i = V_N \\ V_M & \text{if } V_i = V_M \end{cases} \]

Issues in Dynamic Design 2: Charge Sharing

- Charge initially stored on \( C_L \):
  - \( C_A \) previously discharged
- When \( A \) rises, this charge is redistributed (shared) between \( C_L \) and \( C_A \)
- Makes \( \text{Out} \) drop below \( V_{\text{DD}} \)

Solution to Charge Sharing

- Keeper helps a lot
- Can still get failures if \( \text{Out} \) drops below inverter \( V_{\text{sw}} \)
- Another option: precharge internal nodes
- Increases power and area
**Issues in Dynamic Design 3: Clock Feedthrough**

Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above $V_{DD}$. The fast rising (and falling edges) of the clock couple to Out.

**Backgate Coupling Effect**

**Clock Feedthrough**

**Other Effects**
- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)

**Issues in Dynamic Design 4: Backgate Coupling**

Dynamic NAND

Static NAND

**Next Lecture**
- Digital arithmetic
  - Adders
- Domino Logic