Problem 1: Complex CMOS Gates

a) Implement the function \( F = \overline{A} + \overline{B} \cdot (\overline{C} + D) + E \). Assuming long-channel transistors, size the devices so that the drive resistance is the same as an inverter with \( W_N/L = 2 \) and \( W_P/L = 4 \).

b) Imagine that input "A" to the gate was always the last one to arrive, making the delay of the gate from A rising or falling to the output falling or rising critical. Please re-arrange the implementation of your gate so that the delay of the gate from A transitioning is minimized.

c) Re-arrange your gate once again, but this time to minimize the delay of the gate for "D" being the critical input.

d) Draw a stick diagram of the gate you designed for part c) - you should minimize the diffusion breaks and use a single piece of poly for each input.

Problem 2: Wires and Tapering

Use Tables 4-2 and 4-3 from the book for this problem. Also, assume that the sheet resistance of an aluminum wire is \( .075 \Omega/\square \).

a) For an aluminum wire of width 0.24µm on the first layer of metal (Al1) that does not run over any active area and has no other wires above, below, or around it, what is the total capacitance per unit length? What is the resistance per unit length?

b) How long does this same wire need to be for its step input RC delay to be 100ps?

c) If the same 0.24µm wide wire now had two wires on the same layer running parallel to it (with minimum spacing), assuming the parallel wires are both connected to one of the rails, what is the new capacitance per unit length?

d) The wire shown in Figure 1 is on the third metal layer (Al3) and it does not run over any active area. There are no wires close to it and the load attached to the end of the wire has half the capacitance of the first wire section (the one with size \( L \cdot W \)). Assume \( L = 100 \) µm, \( W = 0.7 \) µm, and \( S = 0.7 \). Ignoring fringing capacitance, draw the RC model you would use to calculate the delay of this wire. Using this model, what is the step input RC delay of the wire?
Problem 3: Repeaters

For this problem, use the following parameters for the wire: \( R = 0.075 \, \Omega/\square \), \( W = .1 \, \text{um} \), and \( C = 0.2 \, \text{fF/um} \) (this number includes the effects of both parallel plate and fringe capacitance). For the inverters you should assume that \( V_{dd} = 1.2 \, \text{V} \), \( C_g = 2 \, \text{fF/um} \), \( C_d = 1 \, \text{fF/um} \), \( R_{nmos} = 10 \, \text{k}\Omega/\square \), and \( R_{pmos} = 20 \, \text{k}\Omega/\square \). All of the inverters in Figure 2 are the same size as the first inverter.

Problem: What is the optimal tapering factor (S) that minimizes the delay of the wire?

![Figure 2](image.png)

**Figure 2**

a) Draw an RC model for the above circuit and calculate the delay from the input to \( V_{out} \). You should include slope effect, but you can assume that the input is driven by another circuit with the same delay as first inverter, and that \( \ln(2)*(1+V_T/V_{dd})=1 \). In other words, you can approximate the Elmore delay as being equal to just RC (instead of \( \ln(2)*RC \)).

b) Now assume you have a wire with a total length of \( L \) and that this wire is broken into \( N \) repeated sections with identically sized inverters (where each inverter is a factor of \( S \) bigger than the inverters shown in Figure 2). How does delay depend on \( N \), inverter sizing \( S \), and wire length \( L \)?

c) What \( N \) and \( S \) minimize the delay for a given \( L \)?