PROBLEM 1: Buffer Chains

In this problem you will choose the number of stages and the sizing for the inverter chain shown in Figure 1. Assume that the input capacitance of the first inverter is $C_{\text{unit}}$, $\gamma=0.8$, and $t_{\text{inv}}$ is the unit delay of an inverter as defined in lecture (i.e., $t_p = t_{\text{inv}}(\gamma + f)$).

a) What is the optimal number of stages to use for this inverter chain? (Note that you don’t need to worry about the logical polarity of the signal.)
b) Using your answer to part a), what is optimal delay of the inverter chain?
c) Every time the input transitions, what is the total capacitance that is charged or discharged by this chain? Don’t forget to include the input capacitance of the first inverter in the chain.
d) If you made the last inverter in your chain half of the delay-optimal size (but left everything else the same), what would be the new delay? What is the new total switched capacitance?

![Figure 1](image-url)
PROBLEM 2: Phase Splitter

Phase splitters, like the one shown in Figure 2, are often used to provide complementary signals when only the true form of the signal is available. For example, these circuits can be very useful for decoders. The sizing of the splitter ensures that the outputs have the same delay. For this problem, assume that the total input capacitance (the gate capacitance of the two inverters) is 1, with the relative sizes shown below in Figure 2. For this problem you should assume that $\gamma=1$ and provide the answers to any delay questions in units of $t_{\text{inv}}$.

![Figure 2.](image)

a) What is delay from In to Out1?
b) What is delay from In to Out2?
c) What value of B minimizes the delay from In to Out2? What is the delay with this B?
d) For a given K and the value of B calculated in part c), what value of F makes the delay from In to Out1 equal to the delay from In to Out2?
e) Using the F you found in part d), how does the delay depend on K?
f) Using the results from d) and e), plot the delay as a function of F.
g) **Bonus:** For "reasonable" F, what is the slope of the delay vs. F curve (your answer should have units of $t_{\text{inv}}$)
PROBLEM 3: Complex Gate Delay

In the gate shown in Figure 3., assume that $C_g = 2 \text{ fF/µm}$ and that all transistors are minimum channel length (i.e., a 1µm wide transistor would have a gate capacitance of 2fF), $\gamma=1$, $R_p=20 \text{ kΩ/□}$, and $R_n=10 \text{ kΩ/□}$.

a) If $B = 1$ and $C = 1$, draw the switch model you would use to calculate the delay of the gate when $A$ transitions from zero to 1 (i.e., the output going low).

b) What is the delay of the gate in this case?

c) Repeat parts a) and b) for $A = 1$, $B=0$, and $C$ transitioning from 1 to zero (i.e., the output going high).