What is this class all about?

- Introduction to digital integrated circuit design engineering
  - Will describe models and key concepts needed to be a good digital IC designer

- Models allow us to reason about circuit behavior
  - Allow analysis and optimization of the circuit's performance, power, cost, etc.
  - Understanding circuit behavior is key to making sure it will actually work

- Teach you how to make sure your circuit works
  - Do you want your transistor to be the one that screws up a 1 billion transistor chip?

What will you learn?

- Understanding, designing, and optimizing digital circuits for various quality metrics:
  - Performance (speed)
  - Power dissipation
  - Cost
  - Reliability

Detailed Topics

- CMOS devices and manufacturing technology
- CMOS gates
- Memories
- Propagation delay, noise margins, power
- Combinational and sequential circuits
- Interconnect
- Timing and clocking
- Arithmetic building blocks
- Design methodologies

Practical Information

- Instructor
  - Prof. Elad Alon
    - 565 Cory Hall, 642-0237, elad@eecs
    - Office hours: TuTh 11am-12pm

- TAs:
  - John Crossley, crossley@eecs (OH: Wed. 3-4pm)
  - Abhinav Gupta, agupta@eecs (OH: Mon. 1-2pm)
  - Lingkai Kong konglk@berkeley (OH: Wed. 4-5pm)

- Web page:
  - http://bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141_f08/

Discussions and Labs

- Discussion sessions
  - F 9-10am, Abhinav
  - F 2-3pm, Lingkai
  - M 5-6pm, John
  - Same material in all sessions!

- Labs (353 Cory)
  - M 3-6pm
  - Tu 12-3pm
  - F 10am-1pm

- Please choose one lab session and stick with it!
Your EECS141 Week

<table>
<thead>
<tr>
<th>M</th>
<th>T</th>
<th>W</th>
<th>R</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Off</td>
<td>Class</td>
<td>Off</td>
<td>Lab</td>
</tr>
<tr>
<td>OH</td>
<td>OH</td>
<td>Class</td>
<td>Lab</td>
<td>OH</td>
</tr>
<tr>
<td>OH</td>
<td>OH</td>
<td>OH</td>
<td>Lab</td>
<td>OH</td>
</tr>
<tr>
<td>OH</td>
<td>OH</td>
<td>OH</td>
<td>Lab</td>
<td>OH</td>
</tr>
<tr>
<td>OH</td>
<td>OH</td>
<td>OH</td>
<td>Lab</td>
<td>OH</td>
</tr>
</tbody>
</table>

* Discussion sections will cover identical material

Class Organization

- 9 Assignments
- One design project (with a few phases)
- Labs: 5 software
- 2 midterms, 1 final
  - Midterm 1: Thurs., October 2, evening (TBD)
  - Midterm 2: Tues., November 4, evening (TBD)
  - Final: Sat., December 20, 12:30-3:30pm (TBD)

Grading Policy

- Homeworks: 12%
- Labs: 8%
- Projects: 20%
- Midterms: 30%
- Final: 30%

Some Important Announcements

- Please use the newsgroup for asking questions (ucb.class.ee141)
- Can work together on homework
  - But you must turn in your own solution
- Please don’t bring food/drinks to 353 Cory
- Lab reports due 1 week after the lab session
- Project is done in pairs
- No late assignments
  - Solutions available shortly after due date/time
- Don’t even think about cheating!

Class Material

- Class notes: Web page
- Lab Reader: Web page
- Check web page for the availability of tools

The Web Site

- The sole source of information
  - http://bwrc.eecs.berkeley.edu/icdesign/eeecs141_f08
- Class and lecture notes
- Assignments and solutions
- Lab and project information
- Exams
- Many other goodies …

Print only what you need: Save a tree!
Software

- Cadence
  - Widely used in industry
  - Online tutorials and documentation
- HSPICE for simulation

Getting Started

- Assignment 1: Getting SPICE to work – see web-page
- Due next Thursday, September 4, 5pm
- NO discussion sessions or labs this week.
- First discussion sessions in Week 2
- First software lab in Week 3

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

The First Computer

- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470

The First Computer

- ENIAC - The First Electronic Computer (1946)

The Transistor Revolution

First transistor
Bell Labs, 1948
**The First Integrated Circuits**

- **Bipolar logic**
- **1960's**
- **ECL 5-input Gate**
- **Motorola 1966**

**Intel Core 2 Microprocessor**

- **Intel, 2006.**
- **291,000,000 transistors (143mm²)**
- **3 GHz operation (65nm CMOS technology)**

**Intel 4004 Microprocessor**

- **Intel, 1971.**
- **2,300 transistors (12mm²)**
- **740 KHz operation (10µm PMOS technology)**

**Moore’s Law**

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months.

*Electronics, April 19, 1965.*

**Intel Pentium 4 Microprocessor**

- **Intel, 2005.**
- **291,000,000 transistors (112mm²)**
- **3.8 GHz operation (90nm CMOS technology)**

**Moore’s Law’s Graph**

- Logarithmic graph showing the doubling of transistors on a chip every 18-24 months.

*Electronics, April 19, 1965.*
Evolution in Complexity

Transistor Counts


Power Dissipation Data

Frequency

Cause: Power Density
Not enough cooling...

Not Only Microprocessors

Cell Phone

Digital Cellular Market
(Phones Shipped)
Units 48M 86M 162M 260M 435M

(data from Texas Instruments)

Challenges in Digital Design

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years...
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels
Next Lecture

- Introduce basic metrics for design of integrated circuits – how to measure delay, power, cost, etc.