Announcements

- Homework #5 due Thursday
  - Homework #6 out next week
- Midterm #1 Tues. Oct. 7th, 6:30-8:00pm in 105 Northgate
  - Midterm review session: Monday 11am-12pm, Kroeber 155
- This Thursday's lecture moved to Fri. 3-4:30pm, 521 Cory
  - Elad's Th. office hours moved to Fri. 4:30-5:30pm

Class Material

- Last lecture
  - MOS Transistor Model
- Today's lecture
  - MOS capacitance
- Reading (3.3.2)

Gate Capacitance

- Capacitance (per area) from gate across the oxide is $W\cdot L \cdot C_{ox}$, where $C_{ox} = \varepsilon_{ox}/t_{ox}$
Gate Capacitance

- Distribution between terminals is complex
  - Capacitance is really distributed
    - Useful models lump it to the terminals
  - Several operating regions:
    - Way off, off, transistor linear, transistor saturated

Transistor in Linear Region

- Channel is formed and acts as the other terminal
  - \( C_{GCB} \) drops to zero (shielded by channel)
- Model by splitting oxide cap equally between source and drain
  - Changing either voltage changes the channel charge

Transistor In Cutoff

- When the transistor is off, no carriers in channel to form the other side of the capacitor.
  - Substrate acts as the other capacitor terminal
  - Capacitance becomes series combination of gate oxide and depletion capacitance

Transistor in Saturation Region

- Changing source voltage doesn’t change \( V_{GC} \) uniformly
  - E.g. \( V_{GC} \) at pinch off point still \( V_{TH} \)
- Bottom line: \( C_{GCS} \approx \frac{2}{3} W \cdot L \cdot C_{OX} \)

Transistor In Cutoff (cont’d)

- When \( |V_{GS}| < |V_{T}| \), total \( C_{GCB} \) much smaller than \( W \cdot L \cdot C_{OX} \)
  - Usually just approximate with \( C_{GCB} = 0 \) in this region.
- (If \( V_{GS} \) is “very” negative (for NMOS), depletion region shrinks and \( C_{GCB} \) goes back to ~\( W \cdot L \cdot C_{OX} \))

Transistor in Saturation Region (cont’d)

- Drain voltage no longer affects channel charge
  - Set by source and \( V_{DS, sat} \)
- If change in charge is 0, \( C_{GCCD} = 0 \)
**Gate Capacitance**

- $C_{\text{gate}}$ vs. $V_{\text{GS}}$ (with $V_{\text{DS}} = 0$)
- $C_{\text{gate}}$ vs. operating region

**Diffusion Capacitance**

- Bottom
  - Area cap
    - $C_{\text{bottom}} = C_{\text{O}} L_d W$
  - Sidewalls
    - Perimeter cap
    - $C_{\text{perimeter}} = C_{\text{O}} (2L_d + W)$
- GateEdge
  - $C_{\text{gate}} = C_{\text{O}} W$
  - Usually automatically included in the SPICE model

**Gate Overlap Capacitance**

- $C_O = C_{\text{O}} x_d$
- Off/Lin/Sat $\Rightarrow C_{\text{GSO}} = C_{\text{GDO}} = C_O \cdot W$

**Junction Capacitance (2)**

- Junction caps are nonlinear
- $C_J$ is a function of junction bias
- SPICE model equations:
  - Area $C_J = \text{area} \times C_{J0} / (1 + |V_{DB}|/\phi_B)^{m_J}$
  - Perimeter $C_J = \text{perim} \times C_{JSW} / (1 + |V_{DB}|/\phi_B)^{m_JSW}$
  - Gate edge $C_J = W \times C_{\text{gate}} / (1 + |V_{DB}|/\phi_B)^{m_JSWG}$
- How do we deal with nonlinear capacitance?

**Gate Fringe Capacitance**

- $C_{\text{JFF}}$ not just from metallurgic overlap – get fringing fields too
- Typical value: $\sim 0.2 \text{fF} \cdot \text{W (in } \mu\text{m})/$edge

**Diffusion Capacitance**

- Bottom
  - Area cap
    - $C_{\text{bottom}} = C_O L_d W$
  - Sidewalls
    - Perimeter cap
    - $C_{\text{perimeter}} = C_{\text{O}} (2L_d + W)$
- GateEdge
  - $C_{\text{gate}} = C_{\text{O}} W$
  - Usually automatically included in the SPICE model

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**Linearizing the Junction Capacitance**

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

$$
C_{\text{eq}} = \frac{\Delta Q}{\Delta V_D} = \frac{Q(V_{\text{high}}) - Q(V_{\text{low}})}{V_{\text{high}} - V_{\text{low}}} - K_f C_{\text{O}}
$$

$$
K_f = \frac{-V_{\text{high}}}{V_{\text{high}} - V_{\text{low}}} \left[ \frac{1}{(V_{\text{high}} - V_{\text{low}})^{1-n}} \right]
$$
Capacitance Model Summary

- **Gate-Channel Capacitance**
  - $C_{GQC} = 0$ 
    - $(|V_{GSl}| < |V_T|)$
  - $C_{GQC} = C_{ox} W L_{eff}$ 
    - 50% G to S, 50% G to D
  - $C_{GQC} = (2/3) C_{ox} W L_{eff}$ 
    - 100% G to S

- **Gate Overlap Capacitance**
  - $C_{GSO} = C_{GDO} = C_{ox} W$ 
    - (Always)

- **Junction/Diffusion Capacitance**
  - $C_{eff} = C_{j} L_{S} W + C_{jsw} (2L_{S} + W) + C_{jg} W$ 
    - (Always)

Capacitances in 0.25 µm CMOS Process

<table>
<thead>
<tr>
<th></th>
<th>$C_{G}$ (fF/µm²)</th>
<th>$C_{S}$ (fF/µm²)</th>
<th>$C_{D}$ (fF/µm²)</th>
<th>$K$</th>
<th>$R_{S}$ (Ω)</th>
<th>$R_{D}$ (Ω)</th>
<th>$m_{ac}$</th>
<th>$R_{ac}$ (Ω)</th>
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<tr>
<td>NMOS</td>
<td>0.33</td>
<td>2</td>
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<td>0.8</td>
<td>0.38</td>
<td>0.44</td>
<td>0.9</td>
<td>0.9</td>
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<tr>
<td>PMOS</td>
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<td>0.48</td>
<td>0.8</td>
<td>0.32</td>
<td>0.32</td>
<td>0.9</td>
<td>0.9</td>
</tr>
</tbody>
</table>

Model Calibration - Capacitance

- Can calculate $C_{G}$, $C_{S}$ based on tech. parameters
  - But these models are simplified too
- Another approach:
  - Tune (e.g., in spice) the linear capacitance until it makes the simplified circuit match the real circuit
  - Matching could be for delay, power, etc.

Simplified Model

- Capacitance models important for analysis and intuition
  - But often need something simpler to work with
- Simpler model:
  - Lump together as effective linear capacitance to (ac) ground
  - In most processes: $C_{G0} = C_{D0} = 1.5 - 2fF-W(µm)$

Model Calibration for Delay

- For gate capacitance:
  - Make inverter fanout 4
  - Adjust $C_{load}$ until Delay1 = Delay2
- For diffusion capacitance
  - Replace inverter “A” with a diffusion capacitance load

Delay Calibration

- Why did we need that last inverter stage?
**The Miller Effect**

- As $V_{in}$ increases, $V_{out}$ drops
  - Once get into the transition region, gain from $V_{in}$ to $V_{out} > 1$

- So, $C_{gd}$ experiences voltage swing larger than $V_{in}$
  - Which means you need to provide more charge
  - Makes $C_{gd}$ look larger than it really is

- Known as the “Miller Effect” in the analog world

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**Next Lecture**

- VTCs and Delay revisited