Announcements

- Homework #7 due Thursday
  - Project #1 due next Thurs.
Transition Activity and Power

- Energy consumed in $N$ cycles, $E_N$:

$$E_N = C_L \cdot V_{DD}^2 \cdot n_{0\rightarrow1}$$

$n_{0\rightarrow1}$ – number of $0\rightarrow1$ transitions in $N$ cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f = \left( \lim_{N \to \infty} \frac{n_{0\rightarrow1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\rightarrow1} = \lim_{N \to \infty} \frac{n_{0\rightarrow1}}{N} \cdot f$$

$$P_{avg} = \alpha_{0\rightarrow1} \cdot C_L \cdot V_{DD}^2 \cdot f$$
**Factors Affecting Transition Activity**

- “Static” component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations

- “Dynamic” or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations

**Type of Logic Function: NOR**

Example: Static 2-input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Assume signal probabilities
- \( p_{A=1} = 1/2 \)
- \( p_{B=1} = 1/2 \)

Then transition probability
- \( p_{0 \rightarrow 1} = p_{\text{Out}=0} \times p_{\text{Out}=1} \)
  - \( = 3/4 \times 1/4 = 3/16 \)

If inputs switch every cycle
- \( \alpha_{0 \rightarrow 1} = 3/16 \)
Type of Logic Function: NAND

Example: Static 2-input NAND Gate

Assume signal probabilities
\[ p_{A=1} = 1/2 \]
\[ p_{B=1} = 1/2 \]

Then transition probability
\[ p_{0 \rightarrow 1} = p_{Out=0} \times p_{Out=1} \]
\[ = 3/4 \times 1/4 = 3/16 \]

If inputs switch every cycle
\[ \alpha_{0 \rightarrow 1} = 3/16 \]

Type of Logic Function: XOR

Example: Static 2-input XOR Gate

Assume signal probabilities
\[ p_{A=1} = 1/2 \]
\[ p_{B=1} = 1/2 \]

Then transition probability
\[ p_{0 \rightarrow 1} = p_{Out=0} \times p_{Out=1} \]
\[ = \]

If inputs switch in every cycle
\[ \alpha_{0 \rightarrow 1} = \]
Clock

- Always switches
- Often consumes 25-50% of total power
- Clock gating commonly employed

Problem: Reconvergent Fanout

\[ P(Z = 1) = P(B = 1) \cdot P(X = 1 \mid B=1) \]

Becomes complex and intractable fast
**Inter-Signal Correlations**

Logic without reconvergent fanout

\[ P_{0 \rightarrow 1} = (1 - p_A p_B) p_A p_B \]

Logic with reconvergent fanout

\[ P(Z = 1) = p(C=1 | B=1) p(B=1) \]

\[ p_{0 \rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations
- CAD tools best for performing such analysis

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**Glitching in Static CMOS**

The result is correct, but there is extra power dissipated

Also known as dynamic hazards
**Example: Chain of NAND Gates**

![NAND gate diagram]

**Principles for Power Reduction**

- Most important idea: reduce waste
- Examples:
  - Don't switch capacitors you don't need to
    - Clock gating, glitch elimination, logic re-structuring
  - Don't run circuits faster than needed
    - Power $\alpha V_{DD}^2$ – can save a lot by reducing supply for circuits that don't need to be as fast
    - Parallelism falls into this category
- Let's say we do a good job of that – then what?
## Energy – Performance Space

- Plot all possible designs on a 2-D plane
  - No matter what you do, can never get below/to the right of the solid line
- This line is called “Pareto Optimal Curve”
  - Usually (always) follows law of diminishing returns

## Optimization Perspective

- Instead of metrics like EDP, this curve often provides information more directly
  - Ex1: What is minimum energy for XX performance?
  - Ex2: Over what range of performance is a new technique (dotted line) actually beneficial?
**Key Observation**

- Define the Energy/Performance sensitivity of a parameter, for example:

\[
S_{V_{DD}} = \frac{\partial \text{Energy}}{\partial \text{Perf}} \frac{\partial V_{DD}}{\partial V_{DD}} \quad S_{V_{T}} = \frac{\partial \text{Energy}}{\partial \text{Perf}} \frac{\partial V_{T}}{\partial V_{T}}
\]

- At optimal point, sensitivities to all parameters should be the same (ignoring constraints)
  - Must equal slope of the Pareto optimal curve
  - Otherwise, could trade one parameter for another and end up with lower energy at same performance

**Sensitivity Example**
Sensitivity Example
Next Lecture

- CMOS Scaling