Administrative Stuff

- Discussions start this Friday
- Labs start next week
- Homework #1 is due this Thursday
  - Everyone should have an EECS instructional account
  - Use cory, quasar, pulsar
Last Lecture

- Last lecture
  - Introduction, Moore’s law, future of ICs

- Today’s lecture
  - Introduces basic metrics for design of integrated circuits – how to measure delay, power, cost, etc.

HSPICE Syntax

Simple CMOS inverter

```
.include '/home/ff/ee141/MODELS/gpdk090_mos.sp' TT_s1v

* netlist
Vdd vdd 0 1.2
VIN in 0 PULSE 0 1.2 200ps 100ps 2ns 4ns
M0 out in vdd vdd gpdk090_pmos1V L=100e-9 W=120e-9
M1 out in gnd gnd gpdk090_nmos1V L=100e-9 W=120e-9
RB in base 10K
RC vcc out 1K

*extra control information
.options post=2 nomod .op

* analysis
.TRAN .01ns 3ns .DC VIN 0 1.2 .001 .END
```
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power

Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.

- Recurrent costs - variable
  - proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these proportional to chip area
**Total Cost**

- **Cost per IC**
  
  \[
  \text{cost per IC} = \frac{\text{variable cost per IC}}{\text{volume}} + \text{fixed cost}
  \]

- **Variable cost**
  
  \[
  \text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}
  \]
Die Cost

\[
\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}
\]

From: http://www.amd.com

Wafer size

AMD Athlon

- 8" (200mm) 90nm CMOS
- 12" (300mm) 90nm CMOS
- 12" (300mm) 65nm CMOS

From: http://www.sandpile.org
**Yield**

\[ Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\% \]

\[ \text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}} \]

\[ \text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}} \]

**Defects**

\[ \text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}, \text{ where } \alpha \text{ is approximately } 3 \]

\[ \text{die cost} \propto \frac{1}{\left(\text{die/wafer} \propto \text{die area}^{-1}\right) \left(\text{yield} \propto \text{die area}^{-1}\right)} \propto \text{die area}^4 \]

Cost per Transistor

Fabrication cost per transistor

Reliability

- The real world is analog
  - All physical quantities you deal with as a circuit designer are actually continuous
- Thus, even a “digital” signal can be noisy:

Inductive coupling  Capacitive coupling  Power and ground noise
Noise and Digital Systems

- Circuit needs to work despite “analog” noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined

- Digital system is one where:
  - Discrete values mapped to analog levels and back
  - All the elements (gates) can reject noise
    - For “small” amounts of noise, output noise is less than input noise
  - Thus, for sufficiently “small” noise, the system acts as if it was noiseless

Noise Rejection

- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0

- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output

\[
\begin{align*}
& V_{DD} \quad \text{Gain} = \infty \\
& V_{DD}/2 \quad \text{Gain} = 1 \\
& V_{DD}/2 \quad \text{Gain} = 0 \\
& V_{in} \\
& V_{out}
\end{align*}
\]
More Realistic VTC

VOH = f(VOL)
VOL = f(VOH)
VM = f(VM)

Nominal Voltage Levels

Voltage Mapping

Slope = -1
Slope = -1

Undefined Region
**Definition of Noise Margins**

- **Noise margin high:**
  \[ NM_H = V_{OH} - V_{IH} \]

- **Noise margin low:**
  \[ NM_L = V_{IL} - V_{OL} \]

**Digital Gate Noise Reduction: Regenerative Property**

A chain of inverters

Simulated response
**Regenerative Property (Another View)**

Regenerative

\[ f(v) \]

Non-Regenerative

\[ f(v) \]

There is a modified definition of fan-out for CMOS logic.
Key Reliability Properties

- Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too

- Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain = ∞, margin = \(V_{dd}/2\))
  - Output impedance (ideal: \(R_o = 0\))
  - Input impedance (ideal: \(R_i = ∞\))

Example: An Old-time Inverter

![Inverter Graph](chart.png)
Example: An Old-time Inverter

- $V_{OH} = 3.6V$
- $V_{OL} = 0.4V$
- $V_{IL} = 0.6V$
- $V_{IH} = 2.3V$
- $NM_H = V_{OH} - V_{IH} = 1.3V$
- $NM_L = V_{IL} - V_{OL} = 0.2V$

Performance: Delay Definitions

- $t_{PHL}$
- $t_{PLH}$
- $t_r$
- $t_f$
Fanout of Four (FO4) Delay

- Want a way to characterize the delay of a circuit (roughly) independent of technology
- Most common metric:
  - Delay of an inverter driving four copies of itself ($t_{\text{FO4}}$)

A First-Order RC Network

$$v_{\text{out}}(t) = (1 - e^{-t/\tau}) V$$

$$t_p = \ln(2) \tau = 0.69 \text{ RC}$$

Important model – matches delay of an inverter
**Power Dissipation**

Instantaneous power:
\[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_{t}^{t+T} p(t) dt = \frac{V_{\text{supply}}}{T} \int_{t}^{t+T} i_{\text{supply}}(t) dt \]

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**“Power-Delay” and Energy-Delay**

- Want low power and low delay, so how about optimizing the product of the two?
  - So-called “Power-Delay Product”

- Power-Delay is by definition **Energy**
  - Optimizing this pushes you to go as slow as possible

- Alternative gate metric: **Energy-Delay Product**
  - EDP = \((P_{\text{av}} \cdot t_p) \cdot t_p = E \cdot t_p\)
Energy in CMOS

- The voltage on $C_L$ eventually settles to $V_{DD}$
- Thus, charge stored on the capacitor is $C_L V_{DD}$
  - This charge has to flow out of the power supply
- So, energy is just $Q \cdot V_{DD} = (C_L V_{DD}) \cdot V_{DD}$

Energy (the harder way)

$$E_{0 \rightarrow 1} = \int_0^T P_{DD}(t) \, dt = V_{DD} \int_0^T i_{DD}(t) \, dt = V_{DD} \int_0^{V_{DD}} C_L \, dv_{out} = C_L V_{DD}^2$$

$$E_C = \int_0^T P_C(t) \, dt = \int_0^T v_{out} i_L(t) \, dt = \int_0^{V_{DD}} C_L v_{out} \, dv_{out} = \frac{1}{2} C_L V_{DD}^2$$
Summary

- Understanding the design metrics that govern digital design is crucial
  - Cost
  - Robustness
  - Performance/speed
  - Power and energy dissipation

Next Lecture

- CMOS switch model and how to build gates out of it