Announcements

- Project phase 2 due tomorrow
  - Phase 3 posted tonight

- Homework #8 out Tuesday, due next Tuesday
Midterm review

Project Phase 3
Class Material

- Last lecture
  - Dynamic logic
- Today’s lecture
  - Domino logic
- Reading
  - Chapter 7
**Domino Logic**

Like falling dominos!

**Why Named Domino?**

Like falling dominos!
Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

Domino Logic LE

\begin{align*}
\text{LE}_{\text{in}} \cdot \text{LE}_{\text{in}} = 2 \\
\text{LE}_{\text{in}} \cdot 1 = 1 \\
\text{LE}_{\text{in}} = 1 \\
\text{TL}_\text{LE}_2 = \frac{7}{3}
\end{align*}
**Domino Logic LE (skewed static gate)**

![Diagram]

- \( \text{LE}_{\text{inv}} = \) 
- \( \text{LE}_{\text{inv}} = \) 
- \( \text{PiLE} = \)

**Buffer “Average” LE**

![Diagram]

- \( \text{LE}_{\text{inv}} = \frac{2}{3} \)
- \( \text{LE}_{\text{inv}} = \frac{5}{6} \)
- \( \text{PiLE} = \frac{10}{18} \approx \frac{3}{4} \)

“Average” \( \text{LE} = \sqrt{\frac{10}{18}} \approx \frac{3}{4} \)
Optimal EF/stage with Domino

- Domino buffers are faster than static CMOS inverters
- Is optimal EF/stage for a chain of domino gates still 4?

Designing with Domino Logic

Inputs = 0 during precharge
Can be eliminated
**Footless Domino**

The first gate in the chain needs a foot switch. Precharge is rippling — short-circuit current.

Can mitigate short-circuit current by alternating between footed and unfooted domino.
Footless Domino

To eliminate the short-circuit current, can delay the clock for each stage

Differential (Dual Rail) Domino

Allows inverting gates to be built
**np-CMOS**

Only $0 \rightarrow 1$ transitions allowed at inputs of PDN
Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

**NORA Logic**

Fast, but EXTREMELY sensitive to noise!
Next Lecture

- Flops and Latches