Announcements

- Project phase 2 due tomorrow
  - Phase 3 posted tonight
- Homework #8 out Tuesday, due next Tuesday

Class Material

- Last lecture
  - Dynamic logic
- Today’s lecture
  - Domino logic
- Reading
  - Chapter 7

Midterm review

Domino Logic
**Domino Logic**

- **In1**
- **In2**
- **PON**
- **Clk**
- **Out1**

**Domino Logic LE**

- **In4**
- **PON**
- **Clk**
- **Out2**

**Why Named Domino?**

Like falling dominos!

**Properties of Domino Logic**

- Only non-inverting logic can be implemented
- Very high speed
  - Static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

**Buffer “Average” LE**

- **Domino buffer**
- **LE**
- **“Average” LE**
Optimal EF/stage with Domino

- Domino buffers are faster than static CMOS inverters
- Is optimal EF/stage for a chain of domino gates still 4?

Footless Domino

- Can mitigate short-circuit current by alternating between footed and unfooted domino

Designing with Domino Logic

- Inputs = 0 during precharge
- Can be eliminated
- To eliminate the short-circuit current, can delay the clock for each stage

Footless Domino

- The first gate in the chain needs a foot switch
- Precharge is rippling – short-circuit current

Differential (Dual Rail) Domino

- Allows inverting gates to be built
**np-CMOS**

Only $0 \rightarrow 1$ transitions allowed at inputs of PDN
Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

**NORA Logic**

Fast, but EXTREMELY sensitive to noise!

**Next Lecture**

- Flops and Latches