Announcements

- Project phase 3 out
  - Poster: Wed. Dec. 3rd, 3:30pm in BWRC
  - Report: Mon. Dec. 8th, 5pm in Cory
- Homework #8 out today, due next Tuesday

Why Sequencing?

- Two key (related) reasons that we need sequencing:
  - (1) Want to know when an input has a “new” value

Why Sequential Logic?

- Two key (related) reasons that we need sequencing:
  - (2) Need to slow down signals that are too fast
    - In order to keep them aligned with slower ones
Sequential Elements

- Latch – level sensitive
  - Clk=0: “opaque”
  - Clk-1: “transparent”

- Flip-flop – edge triggered
  - Stores new data when Clk rises

Latch Properties

- Latch transparency can cause data contamination
- Often avoided by using edge-triggered registers
- But have similar issues here too (hold time)

Latches

Use the clock as a decoupling signal, that distinguishes between the transparent and opaque states

Dynamic Latch

Static Latch

Master-Slave Flip-Flop (Edge-Triggered Register)

Two opposite latches create edge-triggered behavior
Also called master-slave latch pair

Static Latch

Forcing the state (can implement as NMOS-only)

Converting into a MUX (gated feedback)

Master-Slave Register

Multiplexer-based latch pair
Reduced Clock Load
Master-Slave Register

More Precise Setup Time

Clk-Q Delay

Setup-Hold Time Illustrations

Setup Time

Setup-Hold Time Illustrations
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data \( T_{\text{Setup}} \) Clock

Time

Hold-1 case

Clock \( T_{\text{Hold}} \) Data

Time
Setup-Hold Time Illustrations

Other Latches/Registers: C²MOS

Other Latches/Registers: TSPC

Including Logic in TSPC

Keepers can be added to staticize

Positive latch (transparent when CLK = 1)
Negative latch (transparent when CLK = 0)

Example: logic inside the latch
AND latch
**Pulse-Triggered Latches**

Ways to design an edge-triggered sequential cell:

- **Master-Slave Latches**
- **Pulse-Triggered Latch**

![Diagram of TSPC Register](image)

![Diagram of Pulsed Latches](image)

**Why not route the pulse?**

![Diagram of HLFF Timing](image)
Next Lecture

- Timing