Announcements
- Homework #8 due today
- Project phase 3
  - Poster session Wed. Dec. 3rd 3:30-5:00pm
  - (No lecture Thurs. Dec. 4th)
  - Final report: Mon. Dec. 8th 5:00pm

Class Material
- Last lecture
  - Timing
- Today’s lecture
  - Clock Distribution
- Reading
  - Chapter 10
Clock Distribution

- Single clock generally used to synchronize all logic on the same chip
  - Need to distribute clock over the entire die
  - While maintaining low skew/jitter
  - (And without burning too much power)

Clock Distribution

- What’s wrong with just routing wires to every point that needs a clock?

More realistic H-tree

- Equal wire length/number of buffers to get to every location

Clock Grid

- No RC matching
- But huge power

H-Tree

Equal wire length/number of buffers to get to every location

Example: DEC Alpha 21164 (1995)

- 2 phase single wire clock, distributed globally
- 2 distributed driver channels
  - Reduced RC delay/skew
  - Improved thermal distribution
  - 3.75nF clock load, 20W power
  - 58 cm final driver width
- Local inverters for latching
- Conditional clocks in caches to reduce power
- More complex race checking
- Device variation
Clock Skew in Alpha Processor

2 Phase, with multiple conditional buffered clocks
- 2.8 nF clock load
- 40 cm final driver width
- Local clocks can be gated “off” to save power
- Reduced load/skew
- Reduced thermal issues
- Multiple clocks complicate race checking

EV6 (Alpha 21264) Clocking
600 MHz – 0.35 micron CMOS

GCLK Skew
(at Vdd/2 Crossings)

GCLK Rise Times
(20% to 80% Extrapolated to 0% to 100%)

EV7 Clock Hierarchy (2002)

Active Skew Management and Multiple Clock Domains
+ widely dispersed drivers
+ DLLs compensate static and low-frequency variation
+ divides design and verification effort
+ DLL design and verification is added work
+ tailored clocks
Clock Animations

- By Phillip Restle (IBM)
  http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html

Next Lecture

- Power distribution, I/O