Announcements

- Project phase 3
  - Poster session tomorrow 3:30-5:00pm
  - Final report: Mon. Dec. 8th 5:00pm

- No HW#9
  - Will post optional problems to help you study for the final

- HKN surveys end of next Tues. lecture
  - Please show up to class

- Final exam:
  - Sat. Dec. 13th, 12:30-3:30, 277 Cory
  - Email me if you need an alternate (earlier) day/time
Class Material

- Last lecture
  - Clock distribution
- Today’s lecture
  - I/O Design
  - Power Distribution

I/O Design
Chip Packaging

- Bond wires (~25µm) are used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large (~100µm in 0.25µm technology), with large pitch (100µm)
- Many chips are 'pad limited'

Pad Frame

Layout

Die Photo
**Bonding Pad Design**

- **Bonding Pad**
  - GND
  - Out
  - In
  - $V_{DD}$
  - 100 $\mu$m

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**Chip Packaging**

- An alternative is ‘flip-chip’:
  - Pads are distributed around the chip
  - The soldering balls are placed on pads
  - The chip is ‘flipped’ onto the package
  - Pads still large
    - But can have many more of them
**ESD Protection**

- When a chip is connected to a board, there is unknown (potentially large) static voltage difference.
- Equalizing potentials requires (large) charge flow through the pads.
- Diodes sink this charge into the substrate – need guard rings to pick it up.

**Pads + ESD Protection**

![Diagram of ESD Protection Circuit]
Power Distribution

Power Supply Impedance

- No voltage source is ideal - ||Z|| > 0
- Two principal elements increase Z:
  - Resistance of supply lines (IR drop)
  - Inductance of supply lines (L·di/dt drop)
**Scaling and Supply Impedance**

- Typical target for supply impedance is to get 5-10% variation of nominal supply (e.g., 100mV for 1V supply)

- In traditional scaling $V_{dd}$ drops while power stays constant

- This forced drastic drop in supply impedance
  - $V_{dd} \downarrow$, $I_{dd} \uparrow \rightarrow |Z_{required}| \downarrow$

- Today’s chips:
  - $|Z_{required}| \approx 1 \text{ m}\Omega$

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**IR Drop Example**

- Intel Pentium 4: ~103W at ~1.275V
  - $I_{dd} = 81$Amps

- For 10% IR drop, total distribution resistance must be less than 1.6mΩ

- On-chip wire $R \approx 20\text{mΩ}/\text{sq. (thick metal)}$
  - Can’t meet R requirement even with multiple, complete layers dedicated to power
  - Main motivation for flip-chip packaging
**Power Delivery**

- Achieving such low impedance requires a lot of resources:
  - ~70% of package pins just for power
  - Top 2-3 (thick) metal layers

**Not Just Impedance - Electromigration**

- On-chip wires: current limited to ~1mA/µm for 5-7 year lifetime
On-Chip Power Distribution

- Power network usually follows pre-defined template (often referred to as “power grid”)

3 Metal Layer Approach (EV4)

3rd “coarse and thick” metal layer added to the technology for EV4 design

Power supplied from two sides of the die via 3rd metal layer
2nd metal layer used to form power grid
90% of 3rd metal layer used for power/clock routing

*Courtesy Compaq*
**4 Metal Layers Approach (EV5)**

- 4th "coarse and thick" metal layer added to the technology for EV5 design
- Power supplied from four sides of the die
- Grid strapping done all in coarse metal
- 90% of 3rd and 4th metals used for power/clock routing

![Diagram of Metal Layers](image)

**6 Metal Layer Approach – EV6**

- 2 reference plane metal layers added to the technology for EV6 design
- Solid planes dedicated to Vdd/Vss
- Lowers on-chip inductance

![Diagram of Metal Layers](image)
**Decoupling Capacitors**

![Diagram illustrating decoupling capacitors](image)

**Decoupling capacitors are added:**

- On the board (right under the supply pins)
- On the chip (under the supply straps, near large buffers)

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**Decoupling Capacitors**

- Under the die

![Image of an Intel processor](image)