Announcements

- Final exam:
  - Sat. Dec. 13th, 12:30-3:30, 277 Cory
- HKN surveys end of class today

Class Material

- Last lecture
  - I/O Design
  - Power Distribution
- Today’s lecture
  - Multipliers
  - Flash and DRAM

Binary Multiplication

\[
\begin{array}{cccccccc}
1 & 0 & 1 & 0 & 1 & 0 & 1 & 1
\end{array}
\times
\begin{array}{cccc}
1 & 0 & 1 & 0
\end{array}
\Rightarrow
\begin{array}{cccccccc}
1 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & 0
\end{array}
\]

Partial products

Result

The Array Multiplier
### The M-by-N Array Multiplier: Critical Path

- Critical Path 1
- Critical Path 2
- Critical Path 1 & 2

\[
 t_{\text{critical}} = \left( \left[ (N-1) + (N-2) \right] \right) t_{\text{carry}} + (N-1) t_{\text{sum}} + t_{\text{out}}
\]

### Wallace-Tree Multiplier

- Partial products
- First stage
- Second stage
- Final adder

### Carry-Save Multiplier

- Vector Merging Adder

\[
 t_{\text{parallel}} = t_{\text{carry}} + (N-1) t_{\text{sum}} + t_{\text{out}}
\]

### Multipliers – Summary

- Optimization constraints different than in binary adder
  - Once again:
    - Need to identify critical path
    - And find ways to use parallelism to reduce it
- Other possible techniques
  - Logarithmic versus linear (Wallace Tree Mult)
  - Data encoding (Booth)
  - Pipelining
- First glimpse at system level optimization

### Wallace-Tree Multiplier

- Partial products
- First stage
- Second stage
- Final adder

### ROM and Flash
Read-Only Memory Cells

Diode ROM  MOS ROM 1  MOS ROM 2

WL  BL

WL  BL

WL  BL

WL  BL

WL  BL

WL  BL

WL  BL

WL  BL

WL  BL

WL  BL

VDD

GND

MOS NOR ROM


VDD

GND

Pull-up devices

MOS NAND ROM

All word lines high by default with exception of selected row

MOS NOR ROM Layout

Programming using the Active Layer Only

Polysilicon

Diffusion

Metal1 on Diffusion

MOS NAND ROM Layout

Cell (8λ x 7λ)

No contact to VDD or GND necessary; drastically reduced cell size

Loss in performance compared to NOR ROM

Floating Gate Transistor

Floating gate

Thin tunneling oxide

n+ source

Control gate

programming p-substrate

n+ drain

Many other options …
Programmable-Threshold

1-Transistor DRAM Cell

Floating-Gate Transistor Programming

DRAM Cell Observations

- 1T DRAM requires a sense amplifier
- Read-out of the 1T DRAM cell is destructive
  - Need refresh
- Lose a $V_{TH}$ when writing a “1” into a DRAM cell
  - Bootstrap the word lines to a higher value than $V_{DD}$

Sense Amp Operation

DRAM
Modern 1T DRAM Cells

Trench Cell

Stacked-capacitor Cell

THE END

- This is just the beginning…