Lecture 3
Transistor Basics and
CMOS Gates

Administrative Stuff

- Discussions start this week (Fri.)
- Labs start next week
  - Everyone should have an EECS instructional account
- Homework #1 is due today
- Homework #2 due next Thursday
Class Material

- Last lecture
  - Basic metrics for IC design
- Today’s lecture
  - Transistor basics
  - Brief introduction to CMOS inverter and gates operation (intro to Chapter 3, 6)
- Reading (2.1-2.2, 3.3.1-3.3.2, 6.1-6.2.1)

What is a Transistor?

An MOS Transistor ↔ A Switch!

- $|V_{GS}| \geq |V_T|
- $R_{on}$
**Switch Model of MOS Transistor**

- For $|V_{GS}| < |V_T|$
- For $|V_{GS}| > |V_T|$

**NMOS and PMOS**

- NMOS Transistor: $V_{GS} > 0$
- PMOS Transistor: $V_{GS} < 0$
MOS Transistors - Types and Symbols

- NMOS Enhancement
- NMOS Depletion
- PMOS Enhancement
- NMOS with Bulk Contact

CMOS Logic
Building an inverter with switches

The CMOS Inverter: A First Glance

![CMOS Inverter Circuit Diagram]
**CMOS Inverter**

**First-Order DC Analysis**

\[
\begin{align*}
V_{in} &= V_{DD} \\
V_{in} &= 0
\end{align*}
\]

- \( V_{OL} = 0 \)
- \( V_{OH} = V_{DD} \)
- \( V_m = f(R_n, R_p) \)

**Simulated Inverter VTC (Spice)**

![Graph showing simulated inverter VTC (Spice)]
CMOS Inverter: DC Properties

- $V_{OH} =$
- $V_{OL} =$
- $V_{IL} =$
- $V_{IH} =$
- $N_{MH} =$
- $N_{ML} =$
- $V_M =$

- $V_{OH} = V_{DD} = 2.5V$
- $V_{OL} = 0V$
- $V_{IL} = 1.05V$
- $V_{IH} = 1.45V$
- $N_{MH} = 1.05V$
- $N_{ML} = 1.05V$
- $V_M = 1.2V$
CMOS Inverter: Transient Response

\[ t_{pHL} = f(\text{Ron}C_L) = 0.69 \, \text{R}_nC_L \]

(a) Low-to-high

(b) High-to-low

Static CMOS Gates

At every point in time (except during the switching transients) each gate output is connected to either \( V_{DD} \) or \( V_{SS} \) via a low resistive path.

The outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods).

(Will contrast this later to dynamic circuit style.)
**Static Complementary CMOS**

![CMOS Diagram]

PUN and PDN are dual logic networks
PUN and PDN functions are complementary

**NMOS Transistors in Series/Parallel Connection**

- Transistor ↔ switch controlled by its gate signal
  - NMOS switch closes when switch control input is high

  ![NMOS Series/Parallel Connections]

  \[ Y = X \text{ if } A \text{ AND } B \]

  \[ Y = X \text{ if } A \text{ OR } B \]

- NMOS transistors pass a “strong” 0 but a “weak” 1
**PMOS Transistors in Series/Parallel Connection**

- PMOS switch closes when switch control is low

\[
\text{NOR} \quad X \quad \begin{array}{c}
A \\
\hline
\end{array} \quad \begin{array}{c}
B \\
\hline
\end{array} \quad Y \\
\quad Y = X \text{ if } \overline{A} \text{ AND } \overline{B} = A + B
\]

\[
\text{NAND} \quad X \quad \begin{array}{c}
B \\
\hline
\end{array} \quad \begin{array}{c}
A \\
\hline
\end{array} \quad Y \\
\quad Y = X \text{ if } \overline{A} \text{ OR } \overline{B} = AB
\]

- PMOS transistors pass a “strong” 1 but a “weak” 0

**Threshold Drops**

\[
\text{PUN} \quad \begin{array}{c}
V_{DD} \\
\hline
S \\
\hline
D
\end{array} \quad 0 \rightarrow V_{DD} \\
\begin{array}{c}
0 \rightarrow V_{DD} - V_{Tn} \\
V_{GS} \rightarrow C_L
\end{array}
\]

\[
\text{PDN} \quad \begin{array}{c}
V_{DD} \\
\hline
D \\
\hline
S
\end{array} \quad V_{DD} \rightarrow 0 \\
\begin{array}{c}
V_{GS} \rightarrow |V_{Tn}| \\
V_{DD} \rightarrow |V_{Tn}|
\end{array}
\]
Complementary CMOS Logic Style

- PUP is the dual to PDN (can be shown using DeMorgan’s Theorems)
  \[
  \overline{A + B} = \overline{AB} \\
  \overline{AB} = \overline{A} + \overline{B}
  \]

- Static CMOS gates are always inverting

\[
\text{AND} = \text{NAND} + \text{INV}
\]

Example Gate: NAND

- PDN: \( G = AB \Rightarrow \text{Conduction to GND} \)
- PUN: \( F = \overline{A + B} = \overline{AB} \Rightarrow \text{Conduction to } V_{DD} \)
- \( G(In_1, In_2, In_3, \ldots) \equiv F(In_1, In_2, In_3, \ldots) \)
Example Gate: NOR

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of a 2 input NOR gate

OUT = A + B

Complex CMOS Gate

OUT = D + A \cdot (B + C)
CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

Next Lecture

- CMOS Manufacturing Process
- Design rules