EE141-Fall 2007
Digital Integrated Circuits

Lecture 3
Transistor Basics and CMOS Gates

Administrative Stuff
- Discussions start this week (Fri.)
- Labs start next week
  - Everyone should have an EECS instructional account
- Homework #1 is due today
- Homework #2 due next Thursday

Class Material
- Last lecture
  - Basic metrics for IC design
- Today’s lecture
  - Transistor basics
  - Brief introduction to CMOS inverter and gates operation (intro to Chapter 3, 6)
- Reading (2.1-2.2, 3.3.1-3.3.2, 6.1-6.2.1)

What is a Transistor?
An MOS Transistor ↔ A Switch!

Switch Model of MOS Transistor

NMOS and PMOS

NMOS Transistor
PMOS Transistor
**MOS Transistors - Types and Symbols**

- NMOS Enhancement
- NMOS Depletion
- PMOS Enhancement
- NMOS with Bulk Contact

**The CMOS Inverter: A First Glance**

- $V_{DD}$
- $V_{CC}$
- $V_{in}$
- $V_{out}$

**CMOS Inverter First-Order DC Analysis**

- $V_{OL} = 0$
- $V_{OH} = V_{DD}$
- $V_{M} = f(R_n, R_p)$

- $V_{in} = V_{DD}$
- $V_{in} = 0$

**Building an inverter with switches**

**Simulated Inverter VTC (Spice)**
**CMOS Inverter: DC Properties**
- $V_{OH} =$
- $V_{OL} =$
- $V_{IL} =$
- $V_{IH} =$
- $N_{MH} =$
- $N_{ML} =$
- $V_M =$

**CMOS Inverter: DC Properties**
- $V_{OH} = V_{DD} = 2.5V$
- $V_{OL} = 0V$
- $V_{IL} = 1.05V$
- $V_{IH} = 1.45V$
- $N_{MH} = 1.05V$
- $N_{ML} = 1.05V$
- $V_M = 1.2V$

**Static CMOS Gates**
At every point in time (except during the switching transients) each gate output is connected to either $V_{DD}$ or $V_{SS}$ via a low resistive path.

The outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods).

(Will contrast this later to dynamic circuit style.)

**Static Complementary CMOS**
- PUN and PDN are dual logic networks
- PUN and PDN functions are complementary

**CMOS Inverter: Transient Response**
\[ f_{PHL} = \frac{1}{f_{NM}} \]

\[ f_{NM} = 0.69 \times R_n \times C_L \]

**NMOS Transistors in Series/Parallel Connection**
- Transistor ↔ switch controlled by its gate signal
- NMOS switch closes when switch control input is high
- NMOS transistors pass a “strong” 0 but a “weak” 1
PMOS Transistors in Series/Parallel Connection

- PMOS switch closes when switch control is low

\[ Y = X \text{ if } A \text{ AND } B = A + B \]

\[ Y = X \text{ if } A \text{ OR } B = \overline{AB} \]

- PMOS transistors pass a "strong" 1 but a "weak" 0

Threshold Drops

\[ V_{DD} \rightarrow 0 \]

\[ 0 \rightarrow V_{DD} - V_{TN} \]

\[ V_{DD} \rightarrow |V_{TN}| \]

Example Gate: NAND

- PDN: \( G = AB \) ⇒ Conduction to GND
- PUN: \( F = \overline{A} + B = \overline{AB} \) ⇒ Conduction to \( V_{DD} \)

\( G(In_1, In_2, In_3, ...) \equiv F(In_1, In_2, In_3, ...) \)

Example Gate: NOR

\[ A + B = \overline{A} \cdot B \]

\[ \overline{A} \cdot B = A + B \]

Complementary CMOS Logic Style

- PUP is the dual to PDN (can be shown using DeMorgan's Theorems)

\[ A + B = \overline{AB} \]

\[ \overline{AB} = A + B \]

- Static CMOS gates are always inverting

\[ \text{AND} = \text{NAND} + \text{INV} \]

Complex CMOS Gate

\[ \text{OUT} = B + A \cdot (B + C) \]
**CMOS Properties**

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

**Next Lecture**

- CMOS Manufacturing Process
- Design rules