Administrative Stuff

- Labs start this week
  - Software lab #2 starts Friday
  - Lab reports due the following week in lab
- Homework #2 due this Thurs.
  - Homework #3 out this Thurs.

Class Material

- Last lecture
  - Transistor Basic
  - Brief intro to CMOS gates
- Today’s lecture
  - CMOS manufacturing process (Ch 2.1, 2.2)
  - Design rules (Ch. 2.3)
- Reading (2.1-2.3)

The Manufacturing Process

For a complete walk-through of the process (64 steps), check the Book web-page

http://bwrc.eecs.berkeley.edu/icBook
**Photo-Lithographic Process**

- Typical operations in a single photo-lithographic exposure (from [Fullman]).

**Patterning of SiO₂**

1. Si-substrate
2. Silicon base material
3. Oxidation
4. Spin, rinse, dry
5. Acid etch
6. Photoresist coating
7. Stepper exposure
8. Development
9. Chemical or plasma etch of SiO₂
10. Final result after removal of resist

**A Modern CMOS Process**

- Dual-Well Shallow-Trench-Isolated CMOS Process

**Advanced Metallization**

- Dual-well shallow trench isolated CMOS Process

**Transistor Layout**

- Cross-Sectional View
- Layout View

**CMOS Process Layers**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Well contact (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

Intra-Layer Design Rules

- Same Potential
- Different Potential

Inter-Layer: Transistor Layout

- Inter-Layer: Vias and Contacts

- Inter-Layer: Well and Substrate
CMOS Inverter Layout

Sticks Diagram

• Dimensionless layout entities
• Only topology is important

Layout Editor

Circuit Under Design

Design Rule Checker

CMOS Inverter
Two Inverters

Share power and ground

Abut cells

Connect in Metal

Next Lecture

- Overview of semiconductor memory