Announcements

- Lab #4 this Fri., next Mon., Tues.
- Homework #4 due today
  - Homework #5 due next Thurs.
- Midterm #1 Tues. Oct. 7th, 6:30-8:00pm in 105 Northgate
Class Material

- Last lecture
  - LE and dynamic power in decoders
- Today’s lecture
  - MOS transistor modeling
    - Will see how to use these models to understand tradeoffs between CMOS gate delay, power, etc.
- Reading (3.3.1-3.3.2)

MOS Transistor
Threshold Voltage: Concept

- With positive gate bias, electrons pulled toward the gate
- With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
- Voltage at which surface inverts: “magic” threshold voltage $V_T$

The Threshold Voltage

Threshold

$$V_T = \varphi_{FB} + 2\varphi_F + \frac{Q_B}{C_{ox}}$$

Depletion charge

$$V_T = V_{T0} + \gamma \cdot \left( \sqrt{2\varphi_F + V_{SS}} - \sqrt{2\varphi_F} \right)$$

Fermi potential

$$\varphi_F = \phi_T \cdot \ln \frac{N_A}{n_i}$$

- $2\varphi_F$ is approximately 0.6V for p-type substrates
- $\gamma$ is the body factor
- $V_{T0}$ is approximately 0.45V for our process
Transistor with Gate and Drain Bias

The Drain Current

- Charge density:
  \[ Q(x) = \]

- Velocity:
  \[ v_n(x) = \]

- Current:
  \[ I_D = \]
Solving the Drain Current

- Integrate along the channel:

Plot of I-V Curve

- Is this really what happens?
**Cause of the Problem**

- Why does the current bend down?

- When \((V_{GS} - V_{TH}) - V_{DS}\) is negative, in our analysis the sign of the carriers changes
  - But transistors don’t actually behave this way

- Look at what really happens to channel charge:

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**Transistor in Saturation**

\[ 0 < V_{GS} - V_T < V_{DS} \]

Transistor in Saturation

- Pinch-off
**Saturation**

- For \((V_{GS} - V_T) < V_{DS}\), the effective drain voltage and current saturate:

\[
V_{DS,\text{eff}} = (V_{GS} - V_T)
\]

\[
I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2
\]

- Of course, real drain current isn’t totally independent of \(V_{DS}\)
  - For example, approx. for channel-length modulation:

\[
I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})
\]

**Modes of Operation**

- **Cutoff:**
  \(V_{GS} - V_T < 0\)
  \(I_D = 0\)

- **Linear (Resistive):**
  \(V_{GS} - V_T > V_{DS}\)
  \(I_D = k_n' \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right] \)

- **Saturation:**
  \(0 < V_{GS} - V_T < V_{DS}\)
  \(I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})\)
Another Way of Looking at This

Cutoff:

\[ V_{GS} - V_T < 0 \quad \Rightarrow \quad I_D = 0 \]

On: (Linear or Saturated)

\[ V_{DS, eff} = \min(V_{GS} - V_T, V_{DS}) \]

\[ I_D = k_n \frac{W}{L} \left[ \left(V_{GS} - V_T\right) \cdot V_{DS, eff} - \frac{V_{DS, eff}^2}{2} \right] \]

Current-Voltage Relations: A Good Ol’ Transistor

![Graph showing current-voltage relations for different gate voltages.]
**Current-Voltage Relations: The Deep Sub-Micron Transistor**

![Graph showing current-voltage relationships](image)

**Velocity Saturation**

- Velocity saturates due to carrier scattering effects

![Graph showing velocity saturation](image)
Velocity Saturation

Long-channel device

Short-channel device

I_D versus V_GS

Long Channel (L=2.5µm)

Short Channel (L=0.25µm)
Including Velocity Saturation

Approximate velocity:

\[ v = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \leq \xi_c \]

\[ = v_{sat} \quad \text{for} \quad \xi \geq \xi_c \]

Continuity requires that:

\[ \xi_c = 2v_{sat}/\mu_n \]

Integrating to find the current again:

\[ I_D = \frac{\mu_n C_{ox}}{1 + (V_{DS}/\xi_c L)} \left[ \left( V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

Velocity Saturation Drain Current

- Saturation occurs when carriers reach \( v_{sat} \)

\[ I_D = W C_{ox} \left( V_{GS} - V_T - V_{DSAT} \right) v_{sat} \]

- We also know that:

\[ I_D = \frac{\mu_n C_{ox}}{1 + (V_{DSAT}/\xi_c L)} \left( \frac{W}{L} \right) \left[ \left( V_{GS} - V_T \right) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right] \]

- Equating the two expressions gives \( V_{DSAT} \) and \( I_D \):

\[ V_{DSAT} = \frac{(V_{GS} - V_T) \xi_c L}{(V_{GS} - V_T) + \xi_c L} \quad I_D = W v_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + \xi_c L} \]
### Regions of Operation

- **Resistive Saturation**
  - \( V_{DS} = V_{GS} - V_{T} \)

- **Velocity Saturation**
  - \( V_{DS} = V_{GS} \cdot V_{T} \)

**Long Channel**
- \( L = 2.5\mu m \)

**Short Channel**
- \( L = 0.25\mu m \)

**W/L = 1.5**

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### Models, Models, Models...

- **Exact behavior of transistor in velocity sat. somewhat challenging if want simple/easy to use models**

- **So, many different models developed over the years**
  - v-sat, alpha, unified, \( V_{T*} \), etc.

- **I often use v-sat model I just presented**
  - Works well for calculating LE of complex gates (more later)
  - But still somewhat complicated – often want even simpler model
Simplified Velocity Saturation

- Assume velocity perfectly linear until hit $\upsilon_{sat}$

\[ \xi_c = \frac{\upsilon_{sat}}{\mu} \]

Simplified Velocity Saturation (cont'd)

- Assume $V_{DSAT} = \xi_c L$ when $(V_{GS} - V_T) > \xi_c L$
### Simplified Model

- Define \( V_{GT} = V_{GS} - V_T \), \( V_{D,VSAT} = \xi_c \cdot L \)

### A Unified Model for Manual Analysis

Define \( V_{GT} = V_{GS} - V_T \)

- For \( V_{GT} \leq 0 \): \( I_D = 0 \)

- For \( V_{GT} \geq 0 \):
  \[
  I_D = k \cdot \frac{W}{L} \cdot \left( V_{GT} \cdot V_{DS,eff} - \frac{V_{DS,eff}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})
  \]
  with \( V_{DS,eff} = \min (V_{GT}, V_{DS}, V_{D,VSAT}) \)
**Simple Model versus SPICE**

![Graph showing Simple Model versus SPICE](image)

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**One Last Simplification**

- If device always operates in velocity sat.:

  \[
  I_D = k \cdot \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{D,FSAT}}{2} \right) V_{D,FSAT}
  \]

- "\(V_T^*\)" model:

  \[
  V_T^* = V_T + \frac{V_{D,FSAT}}{2}
  \]

  \[
  I_D = k \cdot \frac{W}{L} \left( V_{GS} - V_T^* \right) V_{D,FSAT}
  \]

- Good for first cut, simple analysis
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

<table>
<thead>
<tr>
<th></th>
<th>$V_m$ (V)</th>
<th>$\gamma$ (V$^{-2}$)</th>
<th>$V_{th,ar}$ (V)</th>
<th>$n$ (A/V$^2$)</th>
<th>$\lambda$ (V$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$1.15 \times 10^{-6}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-3.0 \times 10^{-4}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

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Next Lecture

- MOS Capacitance