PROBLEM 1: Complex CMOS Gates

For this problem you should use the following parameters for the transistors.

**NMOS:**
L=100nm, $V_{Tn} = 0.25V$, $n = 350 \text{ cm}^2/(\text{V} \cdot \text{s})$, $C_{ox} = 0.95 \text{ F/cm}^2$, $v_{\text{sat}} = 1e7 \text{ cm/s}$, $\lambda = 0$

**PMOS:**
L=100nm, $|V_{Tp}| = 0.25V$, $p = 175 \text{ cm}^2/(\text{V} \cdot \text{s})$, $C_{ox} = 0.65 \text{ F/cm}^2$, $v_{\text{sat}} = 1e7 \text{ cm/s}$, $\lambda = 0$

a) Implement the function $F = \overline{A}(\overline{B} + \overline{C}) + \overline{D}E$. Assuming long-channel transistors, size the devices so that the worst-case drive resistance is the same as an inverter with $W_N/L = 2$ and $W_P/L = 4$.

b) Imagine that input "B" to the gate was always the last one to arrive, making the delay of the gate from B rising or falling to the output falling or rising critical. Please rearrange the implementation of your gate so that the delay of the gate from B transitioning is minimized.

c) Draw a stick diagram of the gate you designed for part b) - you should minimize the diffusion breaks and use a single piece of poly for each input.

d) Now resize the gate to match the worst-case pull-up and pull-down resistances using the velocity saturated model. What is the LE from the B input?

e) Use SPICE to extract the LE from the B input for the gate with the sizing from part d). How does this compare with the result predicted from part d)?

PROBLEM 2: BL Wire for 256x256 SRAM

In this problem we will be looking at a bitline (BL) wire for a 256x256 SRAM array. You should assume that the BL wire is implemented in M2 (which has a minimum width of 0.14µm, $R_w = 0.075 \Omega/\square$) and is running over active. You can also assume that there are no higher metal layers running above it. Right next to this BL, at the minimum allowed distance there is another identical BL (from another cell), as shown on the next page. To calculate the capacitance of this wire, you should use tables 4-2 and 4-3 from the book. You should assume that the cell height is 1µm, that the access device is 120nm wide (which is the minimum width in this technology), and that $C_D = 1.6fF/\mu m$. 

a) What is the total capacitance of the BL due to the BL wires only (i.e. not including the CD of the access devices)?

b) What is the total resistance (from the top of the SRAM to the bottom) of the BL wire?

c) Now including the capacitance of the access devices, what is the total RC delay of the BL wire?

d) How much energy is pulled out of the power supply to charge/discharge the bitlines every time the 256x256 SRAM is read?

**PROBLEM 3: Wire Delay**

In this problem you will calculate the delay of a chain of gates driving a long wire, as shown below. Gate sizes are annotated on the schematic, as are the dimensions of the wire. For the wire parameters you should use: $R = 0.075 \ \Omega/\square$, $W = 0.14 \ \mu m$, $C_{pp} = 6.5 \ aF/\mu m^2$, and $C_{fringe} = 14 \ aF/\mu m$. For the logic gates you should assume that $V_{dd} = 1.2V$, $C_g = 2 \ fF/\mu m$, $C_d = 1.6 \ fF/\mu m$, $R_{nmos} = 10 \ k\Omega/\square$, and $R_{pmos} = 20 \ k\Omega/\square$. Finally, the maximum input capacitance $C_{in} = 8fF$. Note that you should use a minimum channel length of 100nm for the transistors.

![Diagram of gate chain with wire](image)

a) Draw the RC model for calculating the delay of the circuit shown above.

b) Calculate the delay using the model from part a).

c) Without changing the length of the wire, how would you modify the circuit in order to reduce its delay? Draw your improved design and estimate the new delay. (Note that you are allowed to change anything about the circuit except for the length of the wire, $C_{in}$, and $C_L$.)