Announcements

- Project phase 2 out today, due next Fri.

Class Material

- Last lecture
  - Dynamic logic
- Today’s lecture
  - Domino logic
- Reading
  - Chapter 7

Why Named Domino?

Like falling dominos!
Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - Static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

Buffer “Average” LE

Domino Logic LE

Domino Logic LE (skewed static gate)

Optimal EF/stage with Domino

- Domino buffers are faster than static CMOS inverters
- Is optimal EF/stage for a chain of domino gates still 4?

Designing with Domino Logic

Inputs = 0 during precharge

Can be eliminated
The first gate in the chain needs a foot switch. Precharge is rippling – short-circuit current.

Can mitigate short-circuit current by alternating between footed and unfooted domino.

To eliminate the short-circuit current, can delay the clock for each stage.

Only 0 → 1 transitions allowed at inputs of PDN. Only 1 → 0 transitions allowed at inputs of PUN.

Fast, but extremely sensitive to noise!
Next Lecture

- Flops and Latches