EECS 141: FALL 05—MIDTERM 1

Problem 1 (15):
Problem 2 (13):
Problem 3 (12):

Total (40)
PROBLEM 1: VTC, Delay (15 pts)

Consider the digital circuit shown in Fig. 1a. Assume short-channel transistor and you may also assume that all capacitances are constant and linear over the operation range. External load capacitance $C_L = 1\text{fF}$, $V_{DD} = 2.5\text{V}$, $R = 40\text{k}\Omega$. Parameters of NMOS transistor are given below:

\[
\begin{align*}
k' & = 100 \ \mu\text{A/V}^2, \ V_{T0} = 0.5\text{V}, \ V_{DSAT} = 0.5\text{V}, \ \gamma = 0, \ \lambda = 0, \ W / L = 0.5\mu\text{m} / 0.25\mu\text{m} \\
WL \cdot C_{ox} & = 0.6 \ \text{fF}, \ C_{DB} = C_{SB} = 0.1 \ \text{fF}, \ C_{GD,\text{overlap}} = C_{GS,\text{overlap}} = 0.1 \ \text{fF}
\end{align*}
\]

\[\text{Fig. 1a}\]

a. Sketch the VTC for this circuit using the diagram below. Clearly indicate break points and operation modes of transistor $M$ and diode $D$. What is $V_{out}$ when $V_{in} = V_{DD}$? (5 pts)

\[V_{out}(V_{in} = V_{DD}) = \]
b. Calculate the delay of the circuit in Fig. 1a when the input changes from 0 to $V_{DD}$. Let $V_M = 1V$ and assume that $V_{in}$ was at 0 for a long time before the transition. If you are not sure of your answer in (a), assume that the output reaches final value $V_{high} = 1.75V$. What are the equivalent capacitance, equivalent resistance, and the delay? (5 pts)

\[
\begin{align*}
C_{eq} &= \\
R_{eq} &= \\
\tau_p &= 
\end{align*}
\]
c. What is the energy dissipated as heat during high-to-low transition at the output? Assume input voltage step from $V_{DD}$ to 0 and initial $V_{out} = 1.75V$. (1 pt) 

$$E_{diss} =$$

d. For the circuit in Fig. 1b, determine the final value of $V_A$, $V_B$, $V_C$, assuming initial condition at each of the nodes is 3V and $V_{TP} = -0.5V$ (ignore body effect). (2 pts)

![Fig. 1b](image)

$$V_A =$$
$$V_B =$$
$$V_C =$$

e. Assuming that switch closes at time $t = 0$, what is the output voltage at $t = 0^+$ and $t = \infty$ for the circuit in Fig. 1c? $C_L$ was initially discharged, $V_{TP} = -0.5V$. Briefly explain your answer (one line for each point). (2 pts)

![Fig. 1c](image)

$$V_{out} (t = 0^+) =$$
$$V_{out} (t = \infty) =$$
PROBLEM 2: Sizing (13 pts)

Assume the inverters are implemented in standard CMOS with symmetrical VTC. Furthermore, assume $C_{\text{intrinsic}} = C_{\text{gate}} (\gamma = 1)$. Equivalent resistance and input capacitance of unit-sized inverter are $R$ and $C$, respectively. Sizing factor $S \geq 1$.

a. For inverters in Fig. 2a, pick the best sizing factors $S_2$ and $S_3$ to minimize propagation delay. What is the minimum delay (in terms of $t_{p0}$)? (3 pts)

b. What is the total energy drawn from supply when the input switches from 0 to $V_{DD}$? What is the total energy dissipated as heat by the circuit? (Answer in symbolic terms: $C$, $V_{DD}$) (2 pts)
c. For inverters in Fig. 2a (previous page), pick the best sizing $S_2$ and $S_3$ to minimize energy consumption. You may assume square wave at the input with period $T$. What is the total energy consumed for a full cycle (0→1, 1→0)? (3 pts)

$$
S_2 = \\
S_3 = \\
E_{cycle} =
$$

![Fig. 2b](image)

$$
S_2 = 4 \\
S_3 = 6 \\
C_L = 64C
$$

Fig. 2b

d. What is the delay (in terms of $t_{p0}$) of the circuit in Fig. 2b? (2 pts)

$$
t_p =
$$
e. Assume you can choose the sizing $S_2$ and $S_4$ for inverters in Fig. 2c. What are the optimal values for minimum delay? What is the delay (expressed in terms of $t_{pd}$)? (3 pts)

![Fig. 2c](image_url)
PROBLEM 3: General Knowledge (12 pts)

a. Determine the region of operation (Off, Linear, Saturation, Velocity saturation) in the following configurations. You may assume that all transistors are short-channel devices and have identical sizes, $V_{DD} = 2.5V$. Assume following transistor parameters:

NMOS: $V_{Th} = 0.4V$, $k_n = 115 \mu A/V^2$, $V_{DSATn} = 0.6V$, $\lambda = 0$, $\gamma = 0.4V^{1/2}$, $2\Phi_F = -0.6V$

PMOS: $V_{Tp} = -0.4V$, $k_p = -30 \mu A/V^2$, $V_{DSATp} = -1V$, $\lambda = 0$, $\gamma = -0.4V^{1/2}$, $2\Phi_F = 0.6V$

Explain your reasoning and show your derivations if needed. (5 pts)
b. The first row of the table given below lists the characteristics of a successful microprocessor designed for desktop systems. A low power version for portable use is desired and several changes are therefore made to the design. Use simple hand calculations to fill in estimates for blank cells in the table. Use the space below to explain your answers (if needed). All transistors exhibit short-channel I-V characteristics. (5 pts)

<table>
<thead>
<tr>
<th></th>
<th>V_{DD} / V_T (V)</th>
<th>W, L, t_{ox} (relative)</th>
<th>C (nF)</th>
<th>I_{SAT} (mA)</th>
<th>Clock (GHz)</th>
<th>Area (mm^2)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original</td>
<td>2.5 / 0.4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2.4</td>
<td>100</td>
<td>8</td>
</tr>
<tr>
<td>Voltage Scaling</td>
<td>1.25 / 0.2</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>General Scaling</td>
<td>1.25 / 0.2</td>
<td>0.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

c. For each of the following statements, indicate whether it is true or false (circle one answer). (2 pts, 0.5 for correct answer, −0.25 for wrong one)

T   F   (a) The load capacitance of a static CMOS gate has no effect on its VTC.
T   F   (b) The delay of a static CMOS inverter is minimized if (W/L)_p / (W/L)_n = \mu_n / \mu_p.
T   F   (c) Silicided poly lines improve performance by decreasing the capacitance.
T   F   (d) PMOS enters vel. saturation for smaller absolute value of electric field than NMOS.