



EE141-Fall 2010 Digital Integrated Circuits

Lecture 11 MOS Capacitance and Delay

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MOS Capacitance

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Announcements

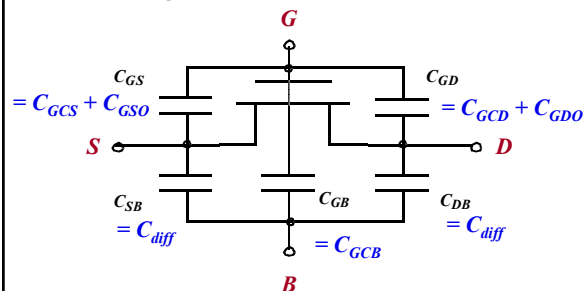
- No lab Fri., Mon.
 - Labs restart next week
- Midterm #1 Thurs. Oct. 7th, 6:30-8:00pm
 - Exam is open notes, book, calculators, etc.

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MOS Capacitances



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Class Material

- Last lecture
 - Using the MOS model: Inverter VTC
- Today's lecture
 - MOS Capacitance
 - Using the MOS Model: Delay
- Reading (3.3.2, 5.4.2)

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Gate Capacitance

- Capacitance (per area) from gate across the oxide is $W \cdot L \cdot C_{ox}$, where $C_{ox} = \epsilon_{ox} / t_{ox}$

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Gate Capacitance

□ Distribution between terminals is complex

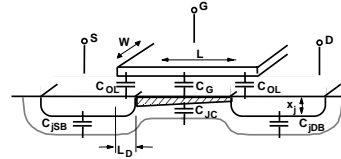
- Capacitance is really distributed
 - Useful models lump it to the terminals
- Several operating regions:
 - Way off, off, transistor linear, transistor saturated

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Transistor in Linear Region



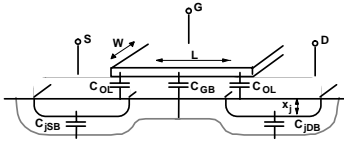
- Channel is formed and acts as the other terminal
 - C_{GCB} drops to zero (shielded by channel)
- Model by splitting oxide cap equally between source and drain
 - Changing either voltage changes the channel charge

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Transistor In Cutoff



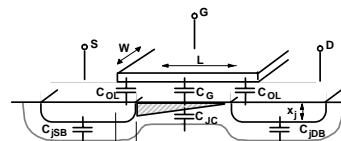
- When the transistor is off, no carriers in channel to form the other side of the capacitor.
 - Substrate acts as the other capacitor terminal
 - Capacitance becomes series combination of gate oxide and depletion capacitance

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Transistor in Saturation Region



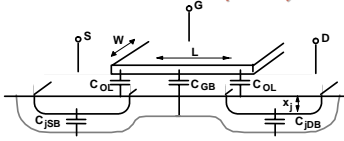
- Changing source voltage doesn't change V_{GC} uniformly
 - E.g. V_{GC} at pinch off point still V_{TH}
- Bottom line: $C_{GCS} \approx 2/3 \cdot W \cdot L \cdot C_{ox}$

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Transistor In Cutoff (cont'd)



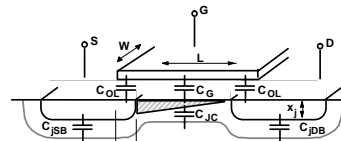
- When $|V_{GS}| < |V_{TH}|$, total C_{GCB} much smaller than $W \cdot L \cdot C_{ox}$
 - Usually just approximate with $C_{GCB} = 0$ in this region.
- (If V_{GS} is "very" negative (for NMOS), depletion region shrinks and C_{GCB} goes back to $\sim W \cdot L \cdot C_{ox}$)

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Transistor in Saturation Region (cont'd)



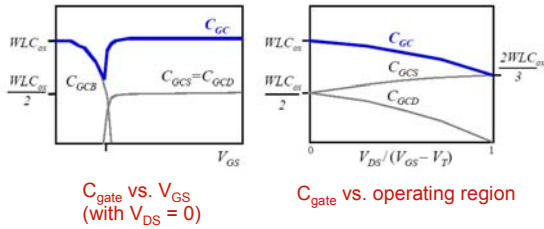
- Drain voltage no longer affects channel charge
 - Set by source and V_{DS_sat}
- If change in charge is 0, $C_{GCD} = 0$

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Gate Capacitance



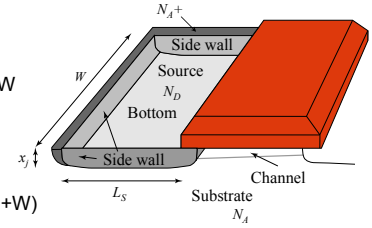
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Diffusion Capacitance

- Bottom
 - Area cap
 - $C_{\text{bottom}} = C_j \cdot L_S \cdot W$
- Sidewalls
 - Perimeter cap
 - $C_{\text{sw}} = C_{j\text{sw}} \cdot (2L_S + W)$
- GateEdge
 - $C_{\text{ge}} = C_{j\text{gate}} \cdot W$
 - Usually automatically included in the SPICE model

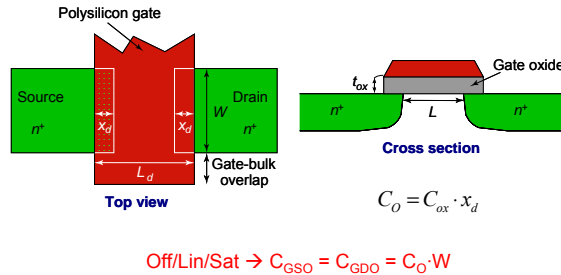


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Gate Overlap Capacitance



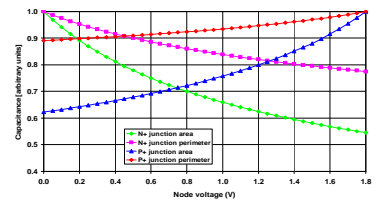
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Junction Capacitance (2)

- Junction caps are nonlinear
 - C_j is a function of junction bias
- SPICE model equations:
 - Area $C_j = \text{area} \times C_{j0} / (1 + |V_{DB}|/\phi_b)^m$
 - Perimeter $C_j = \text{perim} \times C_{j\text{sw}} / (1 + |V_{DB}|/\phi_b)^{m\text{sw}}$
 - Gate edge $C_j = W \times C_{j\text{gate}} / (1 + |V_{DB}|/\phi_b)^{m\text{swg}}$
- How do we deal with nonlinear capacitance?

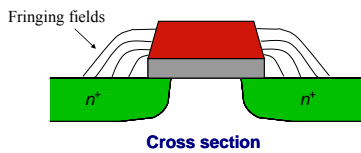


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Gate Fringe Capacitance



- C_{OV} not just from metallurgic overlap – get fringing fields too
- Typical value: $\sim 0.2\text{fF} \cdot W$ (in μm)/edge

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Linearizing the Junction Capacitance

Replace non-linear capacitance by **large-signal equivalent linear capacitance** which displaces equal charge over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_b^m}{(V_{high} - V_{low})(1 - m)} [(\phi_b - V_{high})^{1-m} - (\phi_b - V_{low})^{1-m}]$$

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Capacitance Model Summary

Gate-Channel Capacitance

- $C_{GC} \approx 0$ ($|V_{GS}| < |V_{T1}|$)
- $C_{GC} = C_{ox} \cdot W \cdot L_{eff}$ (Linear)
– 50% G to S, 50% G to D
- $C_{GC} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff}$ (Saturation)
– 100% G to S

Gate Overlap Capacitance

- $C_{GSO} = C_{GDO} = C_O \cdot W$ (Always)

Junction/Diffusion Capacitance

- $C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W) + C_{jg} \cdot W$ (Always)

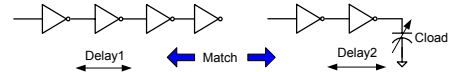
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Model Calibration - Capacitance

- Can calculate C_g , C_d based on tech. parameters
– But these models are simplified too
- Another approach:
– Tune (e.g., in spice) the linear capacitance until it makes the simplified circuit match the real circuit
– Matching could be for delay, power, etc.



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Capacitances in 0.25 μm CMOS Process

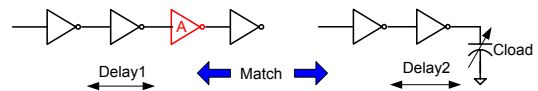
	C_{ox} (fF/ μm^2)	C_O (fF/ μm)	C_j (fF/ μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/ μm)	m_{jsw}	ϕ_{jsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

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Model Calibration for Delay



- For gate capacitance:
– Make inverter fanout 4
– Adjust C_{load} until Delay1 = Delay2
- For diffusion capacitance
– Replace inverter "A" with a diffusion capacitance load

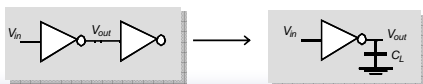
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Simplified Model

- Capacitance models important for analysis and intuition
– But often need something simpler to work with
- Simple switch model:
– Lump together as effective linear capacitance to (ac) ground
– In most processes: $C_G = C_D = 1.5 - 2\text{fF} \cdot W(\mu\text{m})$

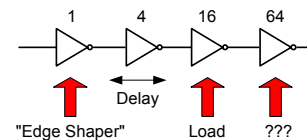


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Delay Calibration



- Why did we need that last inverter stage?

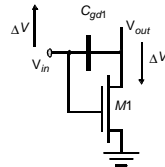
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The Miller Effect

- As V_{in} increases, V_{out} drops
 - Once get into the transition region, gain from V_{in} to $V_{out} > 1$
- So, C_{gd} experiences voltage swing larger than V_{in}
 - Which means you need to provide more charge
 - Makes C_{gd} look larger than it really is
- Known as the "Miller Effect" in the analog world



MOS Transistor as a Switch

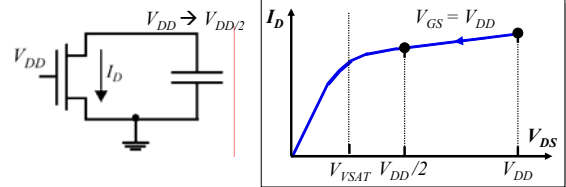
- Saw that real transistors aren't exactly resistors
 - Look more like current sources in saturation
- Two questions:
 - Which region of IV curve determines delay?
 - How can that match up with the RC model?

CMOS Switching Delay



Transistor Driving a Capacitor

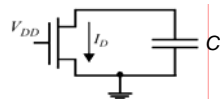
- With a step input:



- Transistor is in (velocity) saturation during entire transition from V_{DD} to $V_{DD}/2$

MOS Transistor as a Switch

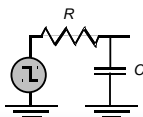
- Discharging a capacitor



$$i_D = i_D(V_{DS})$$

$$i_D = C \frac{dV_{DS}}{dt}$$

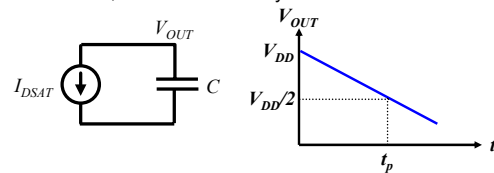
- We modeled this with:



$$t_p = \ln(2) RC$$

Switching Delay

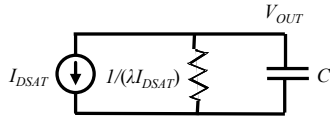
- In saturation, transistor basically acts like a current source:



$$V_{OUT} = V_{DD} - (I_{DSAT}/C)t \longrightarrow t_p = C(V_{DD}/2)/I_{DSAT}$$

Switching Delay (with Output Conductance)

- Including output conductance:



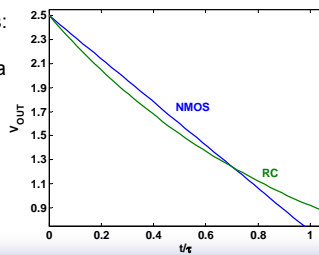
$$V_{OUT} = (V_{DD} + \lambda^{-1}) e^{-t/(C/\lambda I_{DSAT})} - \lambda^{-1}$$

- For "small" λ :
$$t_p \approx \frac{C(V_{DD}/2)}{(1 + \lambda V_{DD}) I_{DSAT}}$$

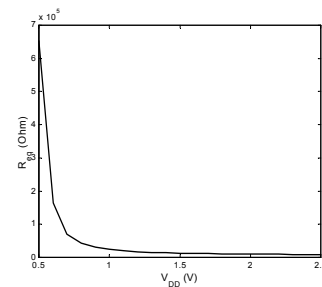
The Book's Method

RC Model

- Transistor current not linear on V_{OUT} – how is the RC model going to work?
- Look at waveforms:
- Voltage looks like a ramp for RC too



The Transistor as a Switch



Finding Req

- Match the delay of the RC model with the actual delay:

$$\frac{C(V_{DD}/2)}{(1 + \lambda V_{DD}) I_{DSAT}} = \ln(2) R_{eq} C \rightarrow R_{eq} = \frac{(V_{DD}/2)}{\ln(2)(1 + \lambda V_{DD}) I_{DSAT}}$$

- Often just:

$$R_{eq} \approx \frac{1}{2 \cdot \ln(2)} \frac{V_{DD}}{I_{DSAT}}$$

- Note that the book uses a different method and gets $0.75 \cdot V_{DD} / I_{DSAT}$ instead of $\sim 0.72 \cdot V_{DD} / I_{DSAT}$.
 - Why did we do it this way vs. the book's method?

The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} ($W/L = 1$) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L .

V_{DD} (V)	1	1.5	2	2.5
NMOS (k Ω)	35	19	15	13
PMOS (k Ω)	115	55	38	31