Schematic and Layout Simulation Exercise

The objective of this laboratory exercise is to walk you through the process of simulating a design and building its layout using previously created components.

At the end of this laboratory exercise, you should be able to:
- Create a layout using instances of existing layout blocks.
- Simulate the extracted layout.

Deliverables for this laboratory exercise: Due at the end of the laboratory session
- Printout of the DRC report showing that your layout is clean.
- Printout of the post-layout simulation results for the CMOS ring oscillator including the transient response, oscillation frequency and average power.

I. Creating the CMOS Ring Oscillator Schematic

Create a new schematic of a 5-stage SMOS ring oscillator, similar to the one below. Use the inverters (symbol view) you created in Lab 2 and create an output pin RingOut (any convenient node will do).

(Don't forget to check and save your schematic before moving on.)

II. Creating the CMOS Ring Oscillator Layout

Create a layout view of the 5-stage ring oscillator by placing 5 instances of the inverter (layout view) that you constructed in Lab 2. Your layout window should look like the image below:
Align the inverter instances such that the power and ground rails are exactly aligned. This should also align the input and output pins, so that your layout window now looks like the following:

To close the ring, use the ‘p’ hotkey to create a path from the rightmost output to the leftmost input. Use the Change To Layer path option to use Metal2 (shown in red below) to avoid shorting the output node to the other Metal1 wires:
Add power and output pins (vdd!, gnd!, and RingOut) to the layout similar to the previous laboratory (The pin names are case-sensitive so make sure the capitalization of pins in schematic matches that in layout).

Note that the pins of the individual inverter layouts will be ignored when the layout is instantiated, so new pins need to be created. This is analogous to local variables in a C-code function wherein these local variables are not visible to the calling function.

After adding the pins, your layout should look like the following:

---

### III. Post-Layout Simulation of the CMOS Ring Oscillator

Now, verify your layout by running DRC and make sure there are no errors. After running DRC, run the circuit extraction and perform LVS. Make sure that the netlists match.
Reminder: the paths for DRC, LVS, and Extraction are

/home/ff/ee141/gpdk090_v3.9/diva/divaDRC.rul
/home/ff/ee141/gpdk090_v3.9/diva/divaLVS.rul
/home/ff/ee141/gpdk090_v3.9/diva/divaEXT.rul

We will now conduct post-layout simulation of this ring oscillator to extract its frequency of operation and measure its average power. So, similar to how you created the SPICE netlist from the extracted view in the last lab, do the same for this ring oscillator.

After extraction, you should see the following: (The numbers for area and perimeter may be different)

Create a new SPICE netlist called `RingOsc.sp` and copy and paste only the transistor instantiations from the extracted SPICE netlist above (This is exactly what you did in the last lab).

Using a power supply of 1.2V, simulate the frequency of this ring oscillator (Note: the oscillator may start in a metastable state, therefore you will need to set initial conditions on the `RingOut` node. You can do so by using the `.IC` statement in SPICE). To measure the frequency, you can simply measure the delay at `RingOut` between when it rises the first time to when it rises the second time. Also, measure the average power dissipated from this structure (You can do this by finding out the average current that comes out from the power supply like you've been doing in your homeworks).

Finally, you should simulate how varying the power supply changes the frequency and average power of the 5-stage Ring Oscillator. So, create a plot of Frequency vs. Power Supply and another of Average Power vs. Power Supply (Vary the power supply from 200mV to 1.2V). Make sure to actually look at the simulated waveforms as you change the power supply and get a rough estimate of the frequency in order to make sure that your
SPICE deck is set up correctly to measure the frequency.

**To be submitted:**

1. Printout showing that your design is DRC clean.
2. Printout of the plots of frequency and average power as a function of the supply voltage.
3. Printout of the ring oscillator layout.

UC Berkeley EE141 Fall 2009
Last Modified: 9/23/09 by Elad Alon