Adding Wires and Other Layers

Before adding other things in your layout, we need to separate the source and drain regions of the NMOS and PMOS transistors by 0.6 microns. This will allow enough distance between these regions and edge of the NWELL region we will define later.

To measure out distances, press the hotkey ‘k’ to create a ruler. Click on the Hide button in the Create Ruler popup window if it appears. Click (do not drag) once on the topmost source or drain diffusion region of the NMOS transistor and move the mouse upward. The ruler will mark of the distance the mouse travels relative to your first click. When the ruler reads 0.6, click once again to create the ruler. Press ESC to exit the ruler creation mode.

Place the mouse over the PMOS transistor. A dashed yellow box appears around the PMOS transistor. To select the PMOS device, left click at this location and the dashed yellow box turns into a solid white ‘selected’ box.

In order to move the PMOS transistor to the correct location, first, zoom in to the PMOS transistor and locate the edge of the PMOS diffusion area. A move consists of three steps:

1. Use the hotkey ‘m’ to enter the ‘move’ command mode. Click on the Hide button in the Move popup window.
2. Position the mouse at the edge of the PMOS diffusion region and click once. This will be the reference point of the move. Notice that moving your mouse moves the PMOS transistor either horizontally or vertically.
3. Move this reference point (in this case, the edge of the PMOS diffusion region) until it is exactly 0.6 microns away from the NMOS diffusion region (refer to the ruler you made earlier). When the PMOS device is at the correct place, click once to finish the move. Press ESC to exit the move command mode.

Note that the rulers will remain in your layout editor window until you delete them using SHIFT-k.

You may want to zoom in to place the starting point of the ruler exactly at the edge of the NMOS diffusion region.
After the move. Notice that the PMOS diffusion region is 0.6 microns away from the NMOS diffusion region.

The hotkey ‘f’ fits the design into the current window. To deselect the PMOS transistor, use CTRL-d.

If the gate of your PMOS transistor is not aligned with the gate of the NMOS transistor, use the ruler and move commands to align them.
To wire up the two gates together, we will use the path command. In the LSW, select the Poly drawing layer, then click on the layout editor window to make it the active window. Then do the following steps:

1. Use the hotkey ‘p’ to enter the path command mode. The Create Path window will open. Make sure that the width field is set to 0.1. Click on the Hide button to hide the Create Path window. 

   Make sure that the layer is set to Poly and the width is set to 0.1.

2. Click on the center of the lower edge of the PMOS gate.

3. Move the mouse to the center of the upper edge of the NMOS gate and double-click. Press ESC to exit the path command mode.

   Make sure that the gates are aligned and that the path you create is also correctly aligned and abutted to both gates. You can check this by using the zoom and pan commands.

We want the inverter to be 1.8 microns wide and 3 microns tall (typical inverter size but not necessarily the smallest you can do with this technology) with the two transistors in the center. Note that with the power rails, this height will increase to 3.6 microns, as we will see later.

To find the center of the inverter, use the ruler you created initially and find the 0.3 mark. Create another ruler from this mark.
horizontally to the center of the Poly path you created. This is the center of the layout.

From this center point, use rulers to outline the edges of the inverter layout.

Use the path command to add the supply (VDD and GND) rails. In the LSW, select the Metal1 layer. Go to the layout editor window and use the ‘p’ hotkey to go into the path command mode. Set the width of the path to 0.6 microns and use the rulers as guides.

Note that the total height of the cell is now 3.6 microns.