Using the path command, wire up the transistors to form your inverter. Your layout should look something like the figure below.

We want to bring the input and output of the inverter to the edge of the layout for easy routing with other blocks later. We also want both the input and output to be on the Metal1 layer. For the output, this is not a problem since the node is already on the Metal1 layer. However, the input is on the Poly layer.

We will use the path command to create a contact from the Poly layer to the Metal1 layer as follows:

1. Select the Poly layer in the LSW.
2. Click on the layout editor window to make it active then press the ‘p’ hotkey. Make sure the width is set to 0.1 and click on the center of the layout (between the two transistors).
3. Halfway between the center of the layout and the left edge of the layout, press F3 to bring up the path popup window. In the Change To Layer pull-down menu, select Metal1. A contact will appear and will be placed when you click on the left mouse button. Click once at approximately halfway between the center and the left edge of the layout.
4. After a contact is placed, move the mouse to the left edge of the layout and double-click to finish. Press ESC to exit the path command mode.

Use a Metal1 width of 0.12 microns for the internal path routing. Use the zoom and pan commands to verify that the wires are aligned correctly.

Since the NMOS and PMOS source and drain regions are not exactly aligned, the output node connection should extend all the way up until the upper edge of the PMOS diffusion contact.
Finish the wiring by creating a path from the output node to the right edge of the layout.

To connect the bulk (substrate) and the Nwell to the appropriate supply rails, substrate/well contacts are used. Use the create instance hotkey ‘i’ and add the M1_PSUB symbolic cell at the center of the bottom supply rail (GND).
Press ESC to exit the Create Instance command mode. Normally, it is desirable to create multiple contacts to the substrate to reduce the contact resistance to the power rails. Select the newly placed M1_PSUB contact and type in the hotkey ‘q’ to edit the contact’s properties. In the Columns field, enter 3 to create 3 contacts instead of 1. Click OK to dismiss the Edit Contact Properties window.
Do the same for the PMOS bulk connection using the **M1_NWELL** contacts to the top supply rail (VDD). Your layout should look similar to the one below.

Note that both the PMOS transistors and the **M1_NWELL** contacts should be inside an **Nwell**. To create the **Nwell**, use the `rectangle` command, as follows:

1. Select the **Nwell** layer in the LSW.
2. In the layout editor window, press the hotkey ‘r’ to enter the `rectangle` command mode. Click the **Hide** button in the `Create Rectangle` popup window.
3. Click (not drag) on the top left corner of the inverter layout to specify the rectangle starting point.
4. Move the cursor to create a rectangle that occupies the upper half the inverter layout. Click to finish.

Your layout should look similar to the one below:

You can use the zoom and pan commands to make sure that the edges of the rectangle coincide with the appropriate corners.