The objective of this introductory laboratory exercise is to walk you through the process of extracting the transistor-level schematic of a layout, verifying the correctness of the layout compared to a schematic, and finally, simulating this extracted circuit.

At the end of this laboratory exercise, you should be able to:
• Add pins to the layout to identify input, output and supply ports.
• Extract the transistor-level schematic of the layout.
• Run the layout-versus-schematic (LVS) tool to verify that the layout and the schematic are topologically equivalent.
• Simulate the extracted schematic.

Deliverables for this laboratory exercise: Due at the end of the laboratory session.
• Printout of the post-layout simulation results for CMOS inverter and the propagation delay times.

I. Adding Pins to the CMOS Inverter Layout

Start up the Cadence IC Front-to-Back (icfb2) tool and open the layout view of the CMOS inverter you made for the previous laboratory exercise.

Select Create → Pin… from the pull down menu to open the Create Symbolic Pin window. In the Terminal Names field, type in the input pin name you used in your schematic (in this case, ‘In’).

Click on the Display Pin Name Option… button and set the Height to 0.2. Then click OK.

Make sure that the Mode is set to ‘sym pin’ and the ‘Display Pin Name’ option is checked.

Set the I/O Type to ‘input’.

The Pin Type should be set to Metal1_T.
Position the symbolic pin exactly on the edge of the input metal path or wire, then left click once to place the symbolic pin. Then move the mouse to place the pin name label (anywhere convenient and easy to see) then left click once again. Your input pin should look similar to the one below.

You can use the zoom and pan keys to place the pin at exactly the right place.

Repeat the same process for the output pin. Note that the I/O Type should be set to 'output'.
The next step is to put in the global power pins. Again, select **Create** → **Pin** … from the pull down menu.

Note that you can put two names in the **Terminal Names** field. This just means that after placing the first pin, you can immediately place the second pin without bringing up the **Create Symbolic Pin** window again.

Note that the **I/O Type** should be set to ‘inputOutput’.

Do not forget the ‘!’ at the end of the power pin names to designate them as global pins.

Place the ‘vdd!’ pin first on the top rail, then place the ‘vdd!’ label at a convenient location, then place the ‘gnd!’ pin, and lastly the ‘gnd!’ label. Your layout should look similar to the one below.
To allow the power pins to connect to the global power pins, you need to edit the power pin properties. Select the vdd! pin and use the hotkey ‘q’ to bring up the Edit Instance Properties window. Click on the Connectivity options and add vdd! to the Net Expression Property and Default fields similar to the one shown below.

Do the same for the gnd! pin, as shown below.
Your final layout with pins should look similar to the one below: