**UNIVERSITY OF CALIFORNIA, BERKELEY**
**College of Engineering**
**Department of Electrical Engineering and Computer Sciences**

**Elad Alon** **Homework #2** **EECS141**

*Due Thursday, September 6, 5pm, box outside 125 Cory*

## PROBLEM 1: VTCs

In this problem we will analyze the noise margins for chains of gates.

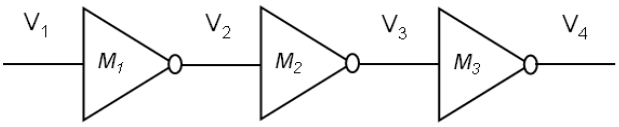



**Figure 1(a)**

a) First, let's consider Figure 1(a). Add to the chain the DC voltage sources that you would use for modeling noise coupling to the input and output of gate $M_2$. You should arrange these voltage sources so that they would both impact the noise margin in the same way (i.e., if the voltage source at the input decreases the noise margin, the voltage source at the output should also decrease the noise margin).

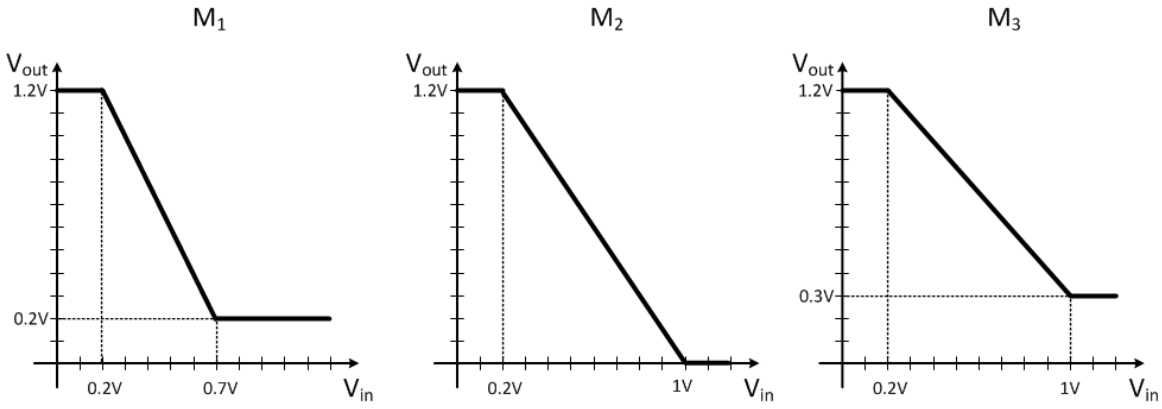



**Figure 1(b)**

b) Figure 1(b) shows the VTC of gates $M_1$, $M_2$, $M_3$, respectively. For each stand-alone gate:
   i. Compute the numerical values in Volts of the noise margins (as defined in class).
   ii. Draw the butterfly diagram of the gate.
   iii. Determine whether the gate is digital or not.

c) Now consider only the cascade of $M_2$ and $M_3$. For this part:
   i. Determine the VTC of the cascade.

ii. Compute the numerical values in Volts of the noise margins (as defined in class).
iii. Determine whether the cascade of the two gates is digital or not.
iv. (BONUS): Given your results to part iii., does every component within a digital system have to be digital, or can you build a digital system out of a combination of digital and non-digital gates?

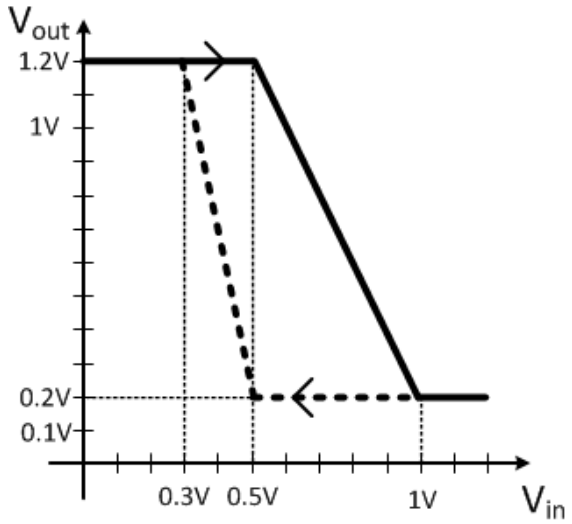
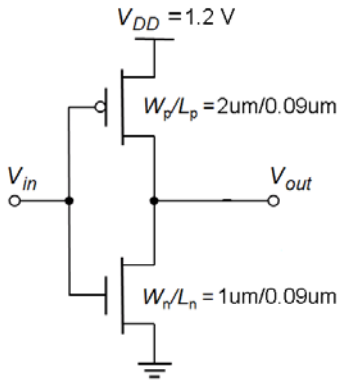



**Figure 1(c)**

d) Now consider a gate with the VTC shown in Figure 1(c). This gate has a hysteretic VTC, meaning that the transition points of its VTC change depending on whether the input voltage is swept from GND to VDD (solid line) or from VDD to GND (dashed line).
   i. Explain (in English) how you would define noise margins in this scenario.
   ii. Compute the numerical values in Volts of the noise margins.

## PROBLEM 2: DELAY

Recall that we have defined the propagation delay $t_p$ as the time between the 50% transition points of the input and output waveforms. In this problem, we will explore how to set up a simulation to measure the propagation time of a digital gate. Please turn in a single spice deck that performs the simulations for parts b) through d). You can measure the delays either by using .MEASURE statements in SPICE, or using WaveView. However, if you use WaveView you should include plots of your waveforms.




a) Create a SPICE subcircuit for the inverter shown above. Use the following line in your SPICE deck to obtain the correct NMOS and PMOS transistor models:

*.LIB '/home/ff/ee141/MODELS/gpdk090_mos.sp' TT_s1v*

To help get you started, we have provided the following example which demonstrates the creation and usage of subcircuits in SPICE. The following input creates an instance named X1 of the MYRC subcircuit, which consists of a 5kΩ resistor and 10fF capacitor in parallel.

*X1 TOP BOTTOM MYRC*

*.SUBCKT MYRC A B*
*R1 A B 5k*
*C1 A B 10f*
*.ENDS*

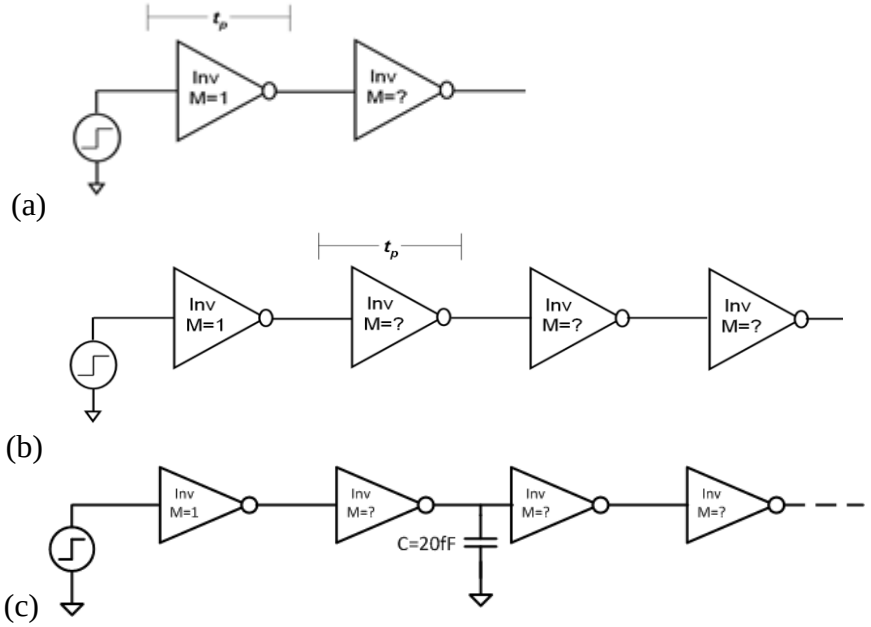



**Figure 2**

b) Measure the average propagation delay of an inverter driving 3 copies of itself (Fig. 2a). First apply a step input with a rise/fall time of 1 ns to the first inverter. Then, repeat this measurement with a rise/fall time of 2 ps. *Note: Use the M (Multiply) parameter in the subcircuit instantiation to replicate the inverter.*

c) Now create a chain of four inverters, each with fanout of 3, as in Figure 2(b). Measure the average propagation delay of the second inverter in the chain when applying a step input to the first inverter (rise/fall time of 1ps). Is the delay from part b) or part c) more realistic in terms of what you might see on an actual IC? Explain the role of the first inverter in the chain.

d) Repeat part c) with the chain of four inverters, each with fanout of 3 (Figure 2(c)), but this time add a 20 fF capacitor to ground (which could be from a wire) between the second and the third inverter. Compare this delay with the result from part c).

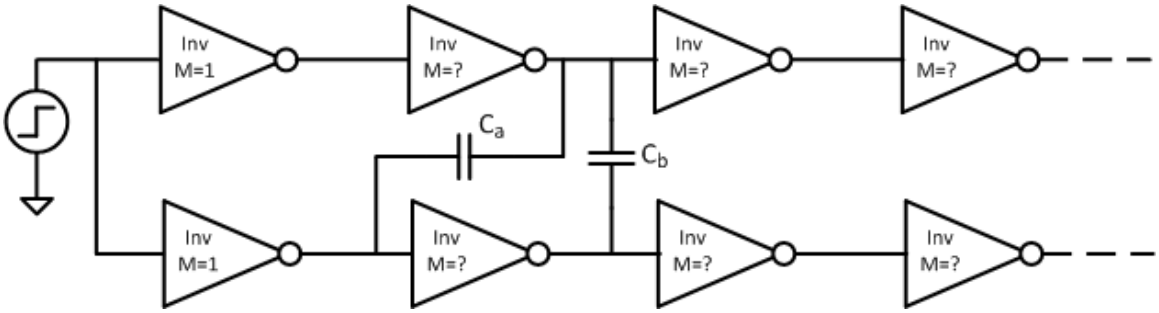



**Figure 2(d)**

e) Now let's use the circuit from Figure 2(d) to see how connecting the capacitor in a different way may have more or less impact on the delay. For each gate, use the fanout of part d). The two rows are identical. For part i) just consider capacitor $C_a$ (disconnect $C_b$), while for part ii) just consider capacitor $C_b$ (disconnect $C_a$).

   i. What value of $C_a$ do you need to use to make the delay of the circuit from Fig. 2d match the delay you measured in part d)? Why might this capacitor be larger or smaller than the 20fF used in part d)?
   ii. Repeat part i) with the new circuit and (briefly) comment on the commonalities/differences between the two behaviors.

## PROBLEM 3: SWITCH MODEL AND ENERGY

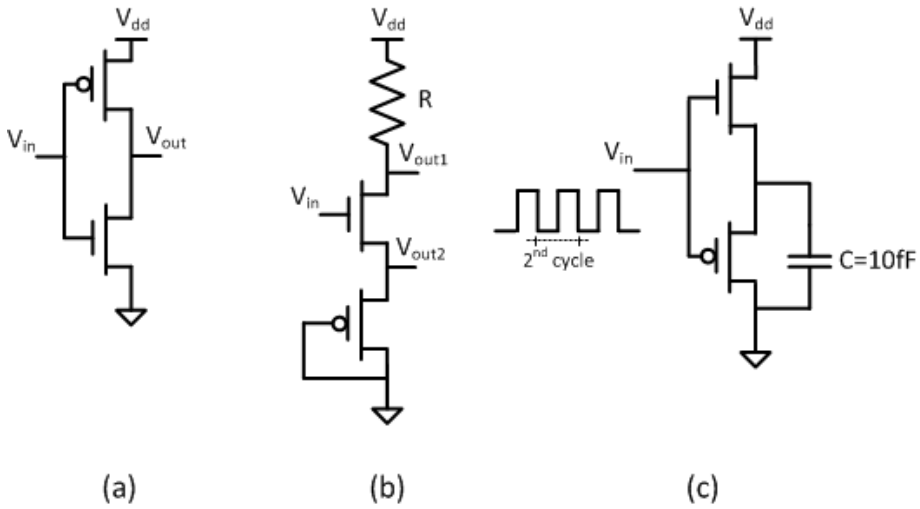



**Figure 3**

In this problem, you should use the simple switch model for MOSFETs.

a) Sketch the VTC for the gate shown in Figure 3(a), assuming $|V_{TP}| = V_{dd}/4$, $V_{TN} = V_{dd}/4$.

b) Now assume $|V_{TP}| = V_{dd}/3$, $V_{TN} = V_{dd}/3$. Sketch the VTC for both outputs of the circuit shown in Figure 3(b) when $R = R_{NMOS} = R_{PMOS}$.

c) Repeat part b) assuming $|V_{TP}| = V_{dd}/6$.

d) Now consider the circuit in Figure 3(c).

   i. Describe the behavior of the gate when the clock signal shown in the figure is applied to its input. In your answer, include both the gate input and output voltage waveforms versus time (with the same time scale). You can assume that at time t=0s the output voltage $V_{out}$=0V. Also, assume that the clock period is $T_{clk}$=10ns and that the RC constant of the gate is much smaller than $T_{clk}$.

   ii. Compute the energy drawn from the supply of the gate during the second clock cycle (as marked in the figure).