

UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

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Homework #3

EE141

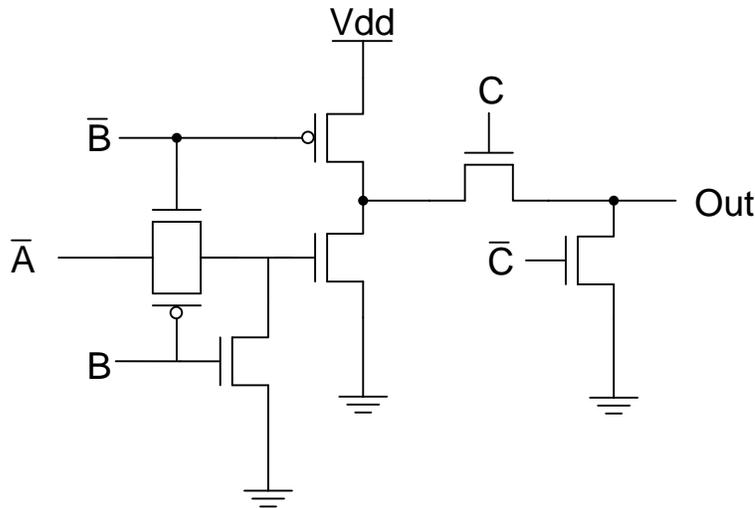
Due Thursday, September 13th, 5pm, box outside 125 Cory

PROBLEM 1: CMOS Logic

- a) Implement the logic function shown below with a static CMOS gate.

$$Out = \overline{ABC} + \overline{ABC} + \overline{ABC}$$

- b) Someone claims they have implemented a static CMOS gate with the circuit shown below. In order to find the problem with this gate, using the switch model, fill in a table showing the voltage (i.e., Vdd, Gnd, Vth, etc.) at Out for all possible combinations of the inputs A, B, and C. In other words, you should fill out the “truth table” for the gate, but with voltages instead of ones and zeros.



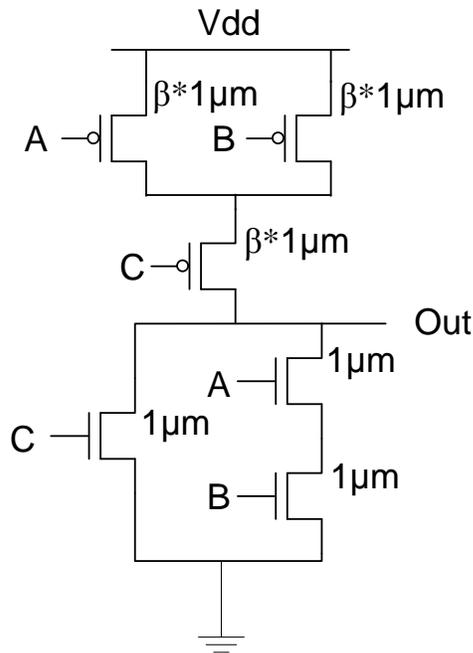
- c) By adding just two more transistors to the circuit shown above, fix the circuit so that it will indeed implement a static gate, with the function shown below. Note that you are free to use both the true and complement versions of the input signals (A, B, and C) to achieve this.

$$Out = (A + B) \cdot C$$

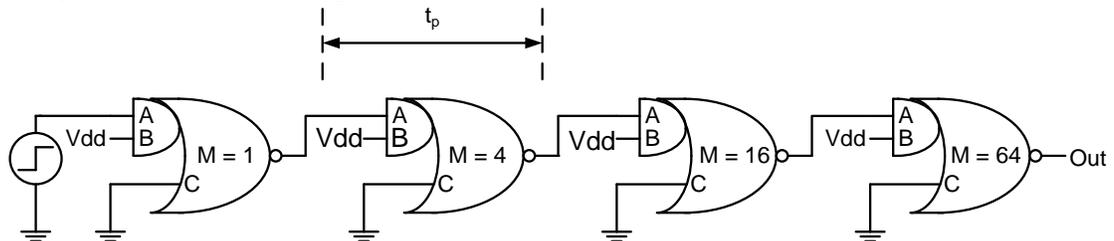
PROBLEM 2: Gate Sizing

Recall that we have defined β as the ratio between the width of the PMOS transistor and NMOS transistor – i.e., $\beta = W_p/W_n$. In this problem we will explore how to optimize β based on different design metrics by using HSPICE. For the following AOI gate, we will use the same sizing for all PMOS transistors in the PUN. Similarly, all the NMOS transistors in the PDN are identically sized. You should make the NMOS transistor $1\mu\text{m}$ wide, and alter the width of the PMOS transistor to change the gate's β ratio. The channel lengths of both the NMOS and PMOS transistors should be fixed at $0.09\mu\text{m}$. This is a good chance to explore HSPICE and use some of its built-in functionality to make this problem easier. (Hint: you'll want to sweep transistor parameters and use .MEASURE statements. Examples will be shown in discussion session.)

- a) Plot V_{IL} and V_{IH} of the AOI gate shown below versus the β ratio, for the A input. In order to measure V_{IL} and V_{IH} , you should assume that the B, C inputs are set to V_{dd} and GND, respectively, and then sweep the A input from 0 to V_{dd} to trace out the VTC.



- b) Sweep β and plot the high-to-low transition delay and the low-to-high transition delay for the second AOI gate in the fanout-of-4 chain shown below.



- c) What β would you use to minimize the **worst case** delay of 3 fanout-of-4 AOI gates? (Hint: The delay characteristics are the same as in part b – you should be able to use the data extracted from there to answer this)
- d) Sweep β and measure the energy and power of this same AOI gate. In this simulation, you should make the input voltage source a 1GHz clock with a 50% duty cycle and 100ps rise/fall time. (An example of how to measure average power and energy using HSPICE will be shown in the discussion session.)

PROBLEM 3: Decoder Warm-up

In this problem, we will implement two decoders using NOR2 and NAND2 gates and inverters and then analyze them to see the effect of the number of inputs on the energy and number of gates. You can use both true and complement forms of the address signals as inputs.

- a) Implement a 2 to 4 decoder by using only NOR2 gates and inverters. Draw the complete schematic and label the inputs and outputs.
- b) Implement a 3 to 8 decoder by using only NOR2 and NAND2 gates. Draw the complete schematic and label the inputs and outputs.
- c) For this part of the problem you should ignore all the junction capacitors from the transistors and assume that each NOR2 and NAND2 gate has 5fF and 4fF of input capacitance, respectively. How much energy is consumed by the above decoder from part b) every time one of the address inputs changes? Note that you shouldn't forget to include the energy consumed by the address inputs.
- d) Now let's compare the energy consumption of the 3:8 decoder from part b) to a design that uses only NAND2 gates and inverters. What is the maximum input capacitance of the inverter for which the NAND2 and inverter only implementation has lower energy consumption than your implementation in part b)? Answer this question for the worst case energy consumption in either design, and use the same input capacitance numbers for the NOR2 and NAND2 gates as in part c).