UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

Elad Alon **Homework #4** **EECS141**

Due Thursday, September 20, 5pm, box outside 125 Cory

PROBLEM 1: Inverter Chains

In this problem you will choose the number of stages and the sizing for the inverter chain shown in Figure 1. You should assume that the input capacitance of the first inverter is C_u, γ=1, and t_{inv} is the unit delay of an inverter as defined in lecture (i.e., $t_p = t_{inv}(\gamma+f)$).

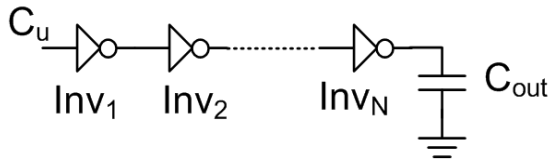

Figure 1.

a) Given that $C_{out} = 2048*C_u$, what is the optimal number of stages to use for this inverter chain? (Note that you don't need to take the logical polarity of the signal into consideration.)
b) Using your answer to part a), what is the optimal delay of the inverter chain?
c) Due to constraints on the specific placement of that inverter in the chip (and how much space is available there), the fourth inverter of the chain must have an input capacitance of $C_{in,4}=128*C_u$ (see Figure 2). Given this new constraint, how would you redesign the chain in order to minimize its overall delay? What is the delay of this new chain?

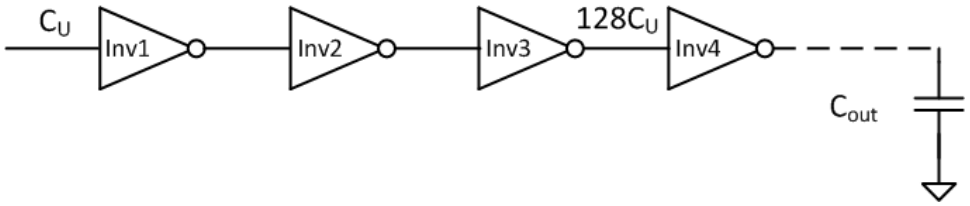

Figure 2

PROBLEM 2: Complex Gate Delay

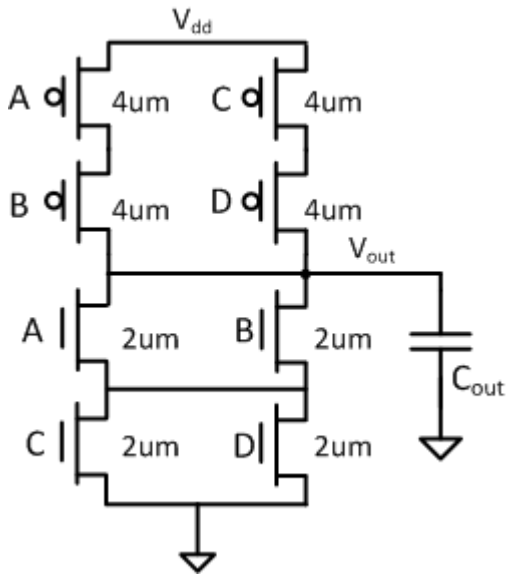

Figure 3.

For this problem you should assume that L_{min} = 100nm, C_g=2 fF/μm, C_D=1.6 fF/μm, R_p=20 kΩ/□, and R_n=10 kΩ/□, C_{out} = 12fF.

a) If B = 0, C=1, D = 0, draw the switch model you would use to calculate the delay of the gate when A transitions from 0 to 1. What are the initial/final values of the output?
b) What is the delay of the gate in this case?
c) Repeat parts a) and b) for A = 1, B=0, D = 0, and C transitioning from 1 to 0.
d) Use HSPICE to simulate the delay of the gate under the conditions from (a) and (c). You can assume that the rise time of the input that is transitioning is 100ps. How well does the simulated delay match with your predictions from (b) and (c)?

PROBLEM 3: Complex Logic and LE

For this problem you should assume that γ=1 and t_{inv} is the unit delay of an inverter as defined in lecture (i.e., $t_p = t_{inv}(\gamma+f)$). You should also express all of your delay answers in units of t_{inv}.

a) Implement the logic function given by the expression shown below as a complex CMOS gate.

$$S = \overline{AB + C(D+E)}$$

b) Assuming the complex gate is sized for equal rise and fall delays, what is the LE of the gate from the A input? What is the LE of the gate from the C input?
c) Now call C_{in} the input capacitance associated with input A. Assuming that C_L = 4,000*C_{in} and that you can add as many inverters as you'd like after the complex

gate (you don't need to maintain the logical polarity at the output), size the chain for the minimum delay for A transitioning and B=1, C=0, D=1, E=0. What is the minimum delay for this design? In terms of C_{in}, what is the total transistor width of all of gates in the chain?

d) Implement the same logic function using only NAND2, NOR2, and inverters. Note that you must place the A input at the very beginning of the chain – i.e., the A input must pass through the largest number of stages.

e) Assuming Cin for the chain from part d) is the same as for part c) and that C_L = 4,000*Cin, size the chain (again, you can add inverters if needed and don't need to maintain the logical polarity) from d) for minimum delay under the same input conditions as part c). What is the minimum delay with this sizing, and what is the total transistor width of all of the gates?

f) Compare the chains from (c) and (e) in terms of delay and total transistor width (which is directly related to power consumption and area) - why is one design faster while the other one is smaller?