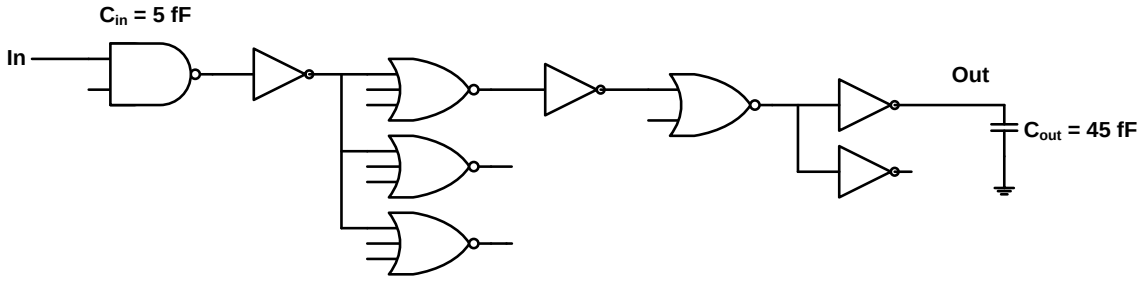
UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

Elad Alon **Homework #5** **EECS141**

Due Thursday, Sept. 27th, 5pm box outside 125 Cory

PROBLEM 1: Logical Effort

For this problem, you should assume that $C_G = 2fF/\mu m$ and that the transistors are long-channel for the purpose of calculating LE.



a) What is the total path effort from IN to OUT?

b) To minimize the delay, what should the EF/stage for this chain of gates be?

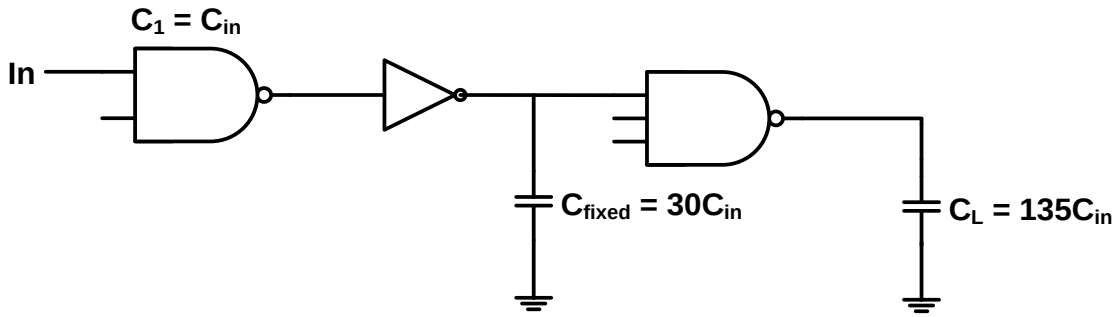
c) Size the gates in this chain to minimize the delay from In to Out. Only calculate the input capacitance of the gates; don't bother to provide the actual transistor sizes.

d) Using this sizing, what is the delay (in units of t_{inv}) of your chain from In rising to Out falling? You can assume that the critical input of the complex gates is always at the "top" of the transistor stacks (i.e., the critical input is always closest to the output node), and that $C_D/C_G = \gamma = 0.5$.

e) You present your design to your boss. She tells you that the team is short on silicon budget, and that you need to cut down on the area of this design. Assuming that area is proportional to the total transistor width and hence input capacitance (note that you should include all transistors in the complex gates), revise your design such that you cut down the area by at least 50%, with a minimum cost in delay. You can assume that you have been provided with the complements of all inputs along the chain (so you don't need to include the area of the gate(s) needed to perform inversion). Compute the delay of the revised design, and find out by how much (in %) does it increase/decrease over the previous design.

PROBLEM 2: Side Loads

We have so far ignored any fixed capacitive load between the gates in a chain, but in a real chip, these devices and gates are connected through metal interconnect. In certain cases, these devices may be placed sufficiently far apart that the delay and power may be affected by the parasitic resistance and capacitance of the wires. For this problem, we'll start by modeling the capacitive component.



Consider the logic chain shown above, where C_{in} = 1fF. There is a fixed (i.e., independent of sizing) capacitance of $C_{fixed} = 30C_{in}$ between the inverter and the final NAND3 gate. This fixed capacitance is sometimes called a side-load.

a) Derive the equation for the delay of this chain in terms of the input capacitances of the three gates (C_1, C_2, C_3), the capacitances C_{fixed} and C_L, γ, and t_{inv}. Assume that the long-channel model is used to size the NAND gates.

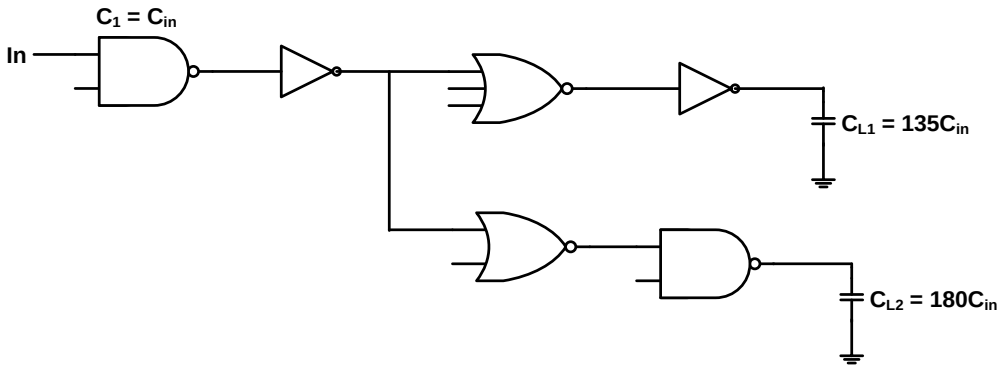
b) Using the values for C_{in} and C_L we have provided and your equation from part a), determine the optimal sizing for the gates to minimize the total delay.

c) We will now explore an alternative heuristic to size the chain. First, pretend that the side-load doesn't exist, and calculate the optimal size for the last NAND gate. Leaving the sizing of this last gate constant and re-introducing the side-load, you can now calculate the total fanout that the first two gates must drive. Based on this total fanout for the first two gates, you can now size the inverter using the standard method we learned in class. Show your work and include a sized gate-level schematic of the new chain.

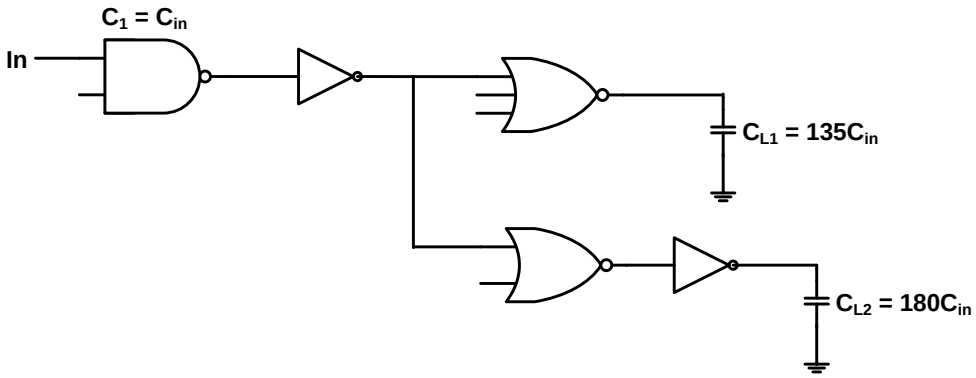
d) In terms of t_{inv}, what is the delay of the chain from part b)? How does this compare to the delay of the chain in part c)? You may assume γ=1. How do the two designs compare in terms of total transistor width?

e) Now let's look at another common situation that will occur in realistic chip designs. In this case, instead of a fixed wire side load, as shown in the figure on the next page, we have a different chain of logic, driving a different final load capacitance. Both of these paths are potentially equally critical in terms of setting the overall performance of the system, and so in general the delay-optimal

solution will size both sub-chains to have equal delay (since making one faster would slow down the other, making it the critical path). Size the gates shown in the figure for optimal delay while keeping the delay of the sub-chains which occur after the split equal. Note that in this particular case, each sub-chain after the split has equal parasitic delay.

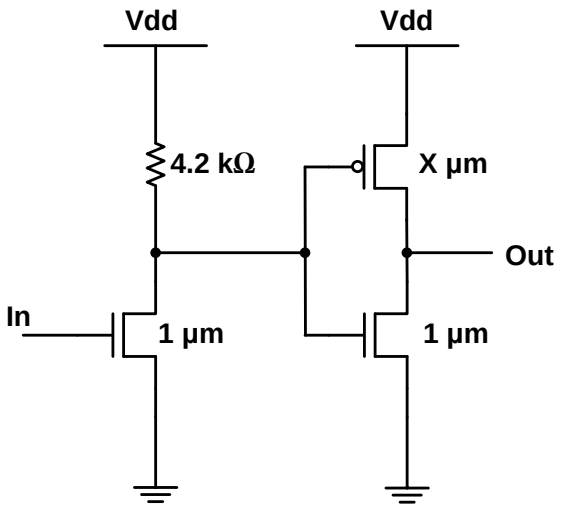


f) [BONUS:] Now let's look at a split in which the number of gates in each sub chain is not equal. Again, we want to size the chain for optimal delay while keeping the delay of sub-chains after the split equal. Note again that the parasitic delay in each branch is equal. Also note that getting some actual numbers for the sizes of the gates will likely require you to solve some equations numerically, and that the majority of the extra credit will be given for setting up equations correctly.



PROBLEM 3: MOS Transistor Model

Use the velocity saturation model presented in lecture (shown below) to complete a) and b). For part c) and d), attach your SPICE netlist and results.
Use L = 100nm, V_{TN} = 150mV, $|V_{TP}|$ = 300mV, υ_{SATN} = 1.12e7 cm/s, υ_{SATP} = 1e7 cm/s, C_{OX} = 15fF/μm^2, μ_N = 260 cm^2/(V·s), μ_P = 120 cm^2/(V·s). Assume V_{dd} = 1.2 V.



$$I_D = W\upsilon_{SAT}C_{OX}\frac{(V_{GS}-V_T)^2}{(V_{GS}-V_T)+\xi_c L}$$

a) Using the model, find I_{DN} of the NMOS in the second inverter when In = 0V and Out = 1.2V. (Note that as we will see later on in the lectures, the current of the transistors in this situation directly impacts the delay of the inverter.)

b) Choose X such that I_{DP} equals the value you got for I_{DN} in part a) when In = 1.2V and Out = 0V.

c) Simulate the circuit with your sizing from b), and compare your results for I_{DP} and I_{DN} from parts a) and b).

d) Explain where any discrepancy between your calculated current and the value you got using SPICE in part c) might come from. Then, use SPICE to find a new value for X that makes the currents match.

e) [BONUS:] Can you make the analytical model fit the SPICE model better by extracting an additional parameter? If so, extract this parameter and recalculate the drain currents using this improved model.