Elad Alon                     **Homework #6**                     **EECS141**
*Due Thursday, October 11, 5pm, box outside 125 Cory*

Unless otherwise noted, you should assume the following parameters for all of the problems in this homework:

**NMOS:**
L=100nm, $V_{Tn}$ = 0.25V, $\mu_n$ = 350 cm$^2$/(V·s), $C_{ox}$ = 0.95 µF/cm$^2$, $v_{sat}$ = 1e7 cm/s, $\lambda$ = 0

**PMOS:**
L=100nm, $|V_{Tp}|$ = 0.25V, $\mu_p$ = 175 cm$^2$/(V·s), $C_{ox}$ = 0.65 µF/cm$^2$, $v_{sat}$ = 1e7 cm/s, $\lambda$ = 0

**PROBLEM 1: RC Model Extraction**

In this problem, you will use the built-in optimization tool in HSPICE to do device characterization. The discussion sessions will cover the syntax needed to perform optimizations in HSPICE, so be sure to attend if you have not used this HSPICE feature before.

a) Using the calibration procedure similar to the one described in class (i.e. Lecture #11 page 21-23), find the linear gate capacitance per µm of transistor width ($C_G$) and the linear drain capacitance per µm of transistor width ($C_D$) that best matches the delay of an inverter. All of the inverters in your calibration circuits should use 100nm long transistors and a $\beta$ of 1.5. Further, you should extract the $C_D$ for the NMOS and the PMOS transistors simultaneously (hint: remember to use the appropriate $\beta$ factor). Perform the simulations using Vdd = 1.2V, 1.0V, 0.8V and 0.6V and plot $C_G$ vs. Vdd and $C_D$ vs. Vdd.

b) Repeat part a), but calibrate both $C_D$ and $C_G$ for energy instead of delay. In addition, plot the average energy pulled from the supply per transition vs. $V_{DD}$. Note that to extract energy, we recommend that you use a 1GHz clock as the input to your inverter chains.

c) Now let's assume that we have a chain of 4 inverters where the third inverter is powered from Vdd=0.8V, whereas the rest of the chain is powered from Vdd=1.2V. Using the capacitance values extracted from part b), calculate the average dynamic power dissipated by the chain for a 1GHz clock input.

d) Knowing that you're interested in the specific situation from part c), how might you modify your calibration procedure to obtain more accurate results for average dynamic power?

## PROBLEM 2: Transistor Capacitance and I-V Curves

a) For this problem you should assume that the total gate capacitance of a minimum length transistor follows the curve shown below (all of the transistors in this problem are minimum length). Although in reality this total gate capacitance is divided between all of the other terminals (source, drain, and body), for simplicity we will assume that all of the gate capacitance goes to the source of the transistor.
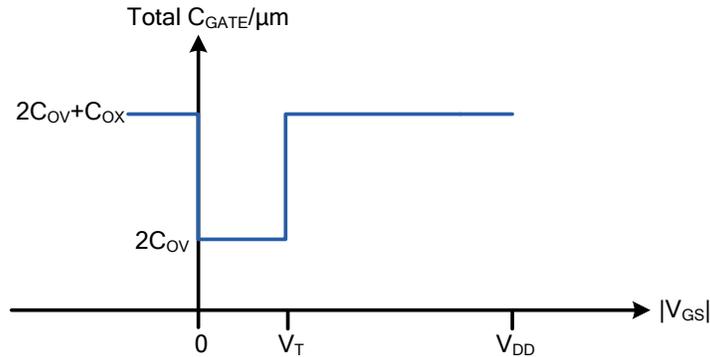


Now assume that the A input of a NOR gate is driven by an inverter as shown in Figure 2(a) and $V(B) = 0$. How much energy is pulled out of the inverter's supply voltage (i.e., $V_{DD,drive}$, whose value is the same as $V_{DD}$) and from $V_{DD}$ in order to charge A from $V_{DD}$ to 0? All of your answers should be provided in terms of $C_{ov}$, $C_{ox}$, $V_T$, and $V_{DD}$.
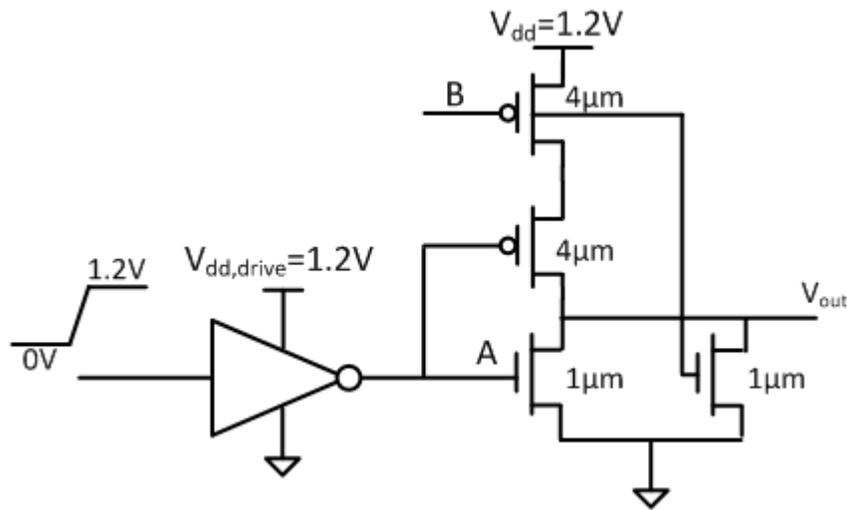


Figure 2(a)

b) Now let's instead assume that $V(B) = V_{DD}$. In this situation, how much energy is pulled out of the inverter's supply voltage and from $V_{DD}$ in order to charge A from $V_{DD}$ to 0?

For parts c) through e), you should use the velocity saturated model for transistor current and ignore all capacitors associated with the transistors – i.e., you can ignore all capacitors except those explicitly drawn in the circuit. Also, $V_{DD} = 1.2V$.

c) Estimate the delay of the inverter shown in Figure 2(b) with an input rising step (i.e., IN = 0 → $V_{DD}$) for $V_{DD} = 1.2V$, 1V, and 0.8V.
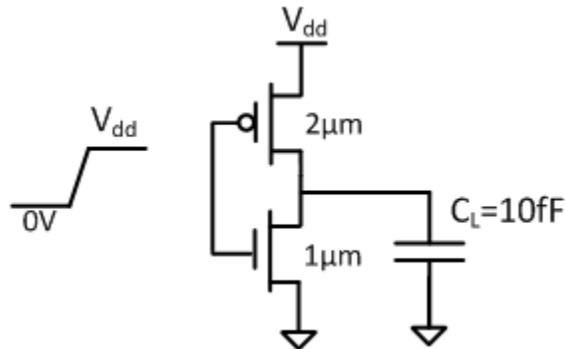


Figure 2(b)

d) Repeat part c) for the NAND2 gate shown in Figure 2(c). Comment on any differences between the delay vs. supply voltage trend for this NAND gate as opposed to the inverter.
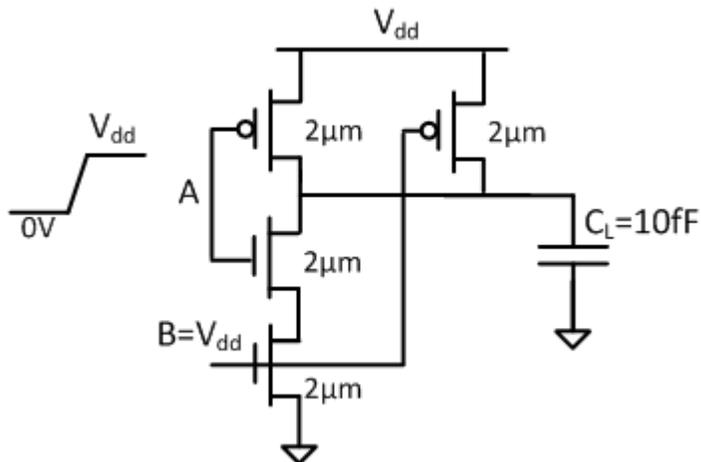


Figure 2(c)

**PROBLEM 3: Power and Delay**

Throughout this problem, you should ignore all the capacitors associated with the transistors – i.e., you can assume that the only capacitors are those explicitly shown in the circuit. Also, you can ignore shoot-through current, and you can assume that the leakage

current is equal to $\frac{W}{L}I_0 e^{\left(\frac{-V_T}{1.5\times25\ mV}\right)}$, where $I_{0,NMOS}=4\mu A$, $I_{0,PMOS}=2\mu A$. And Vdd=1.2V.

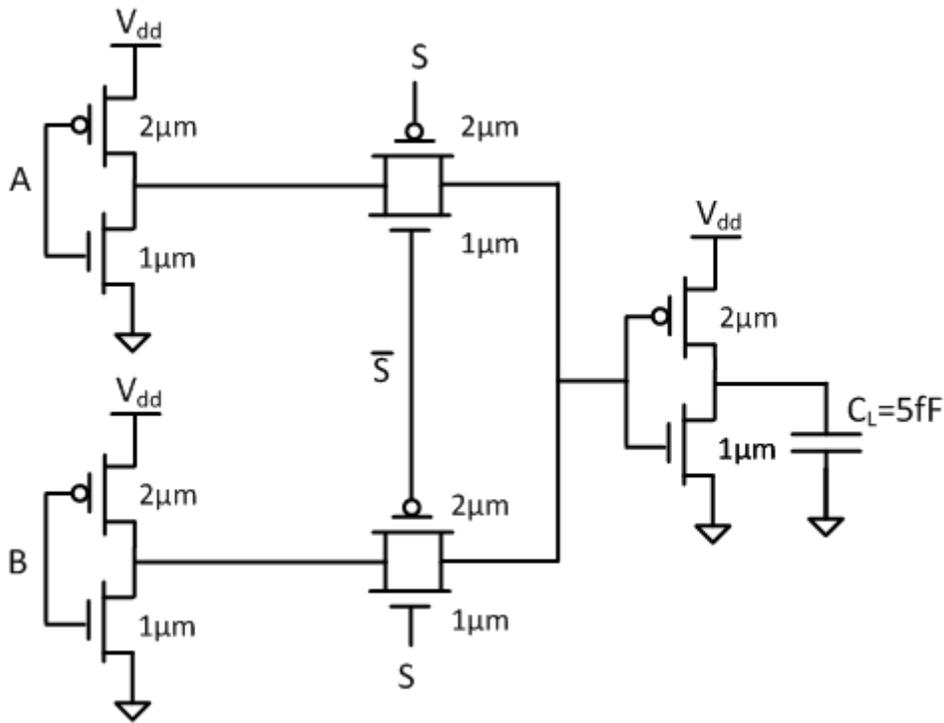Now consider the 2-input transmission gate MUX shown below:



Figure 3(a)

a) Calculate the leakage current for all 8 possible states of the 3 inputs A, B, and S.

b) Assuming that B = 0V and that inputs A and S are driven with the waveforms shown below in Figure 3(b), which repeat every 3ns, calculate the average dynamic power drawn from the supply.
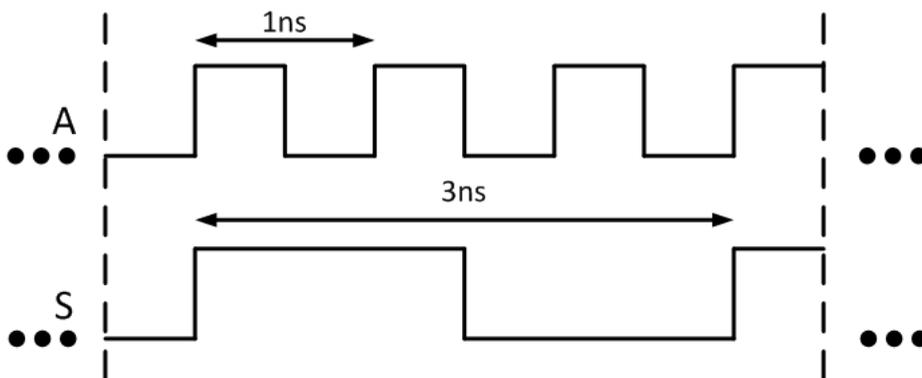


Figure 3(b)

c) Calculate the average total power drawn from the supply with the same inputs shown in part b).