UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

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Due Thursday, October 18, 5pm, box in 240 Cory

PROBLEM 1: Complex CMOS Gates

For this problem you should use the following parameters for the transistors.

NMOS:
L=100nm, V_{Tn} = 0.25V, μ_n = 350 cm^2/(V·s), C_{ox} = 0.95 μF/cm^2, v_{sat} = 1e7 cm/s, $\lambda = 0$
PMOS:
L=100nm, $|V_{Tp}|$ = 0.25V, μ_p = 175 cm^2/(V·s), C_{ox} = 0.65 μF/cm^2, v_{sat} = 1e7 cm/s, $\lambda = 0$

a) Implement the function $F = \overline{A(B+C)(C+E)}$. Assuming long-channel transistors, size the devices so that the worst-case drive resistance is the same as an inverter with $W_N/L = 2$ and $W_P/L = 4$.

b) Imagine that input "B" to the gate was always the last one to arrive, making the delay of the gate from B rising or falling to the output falling or rising critical. Please re-arrange the implementation of your gate so that the delay of the gate from B transitioning is minimized.

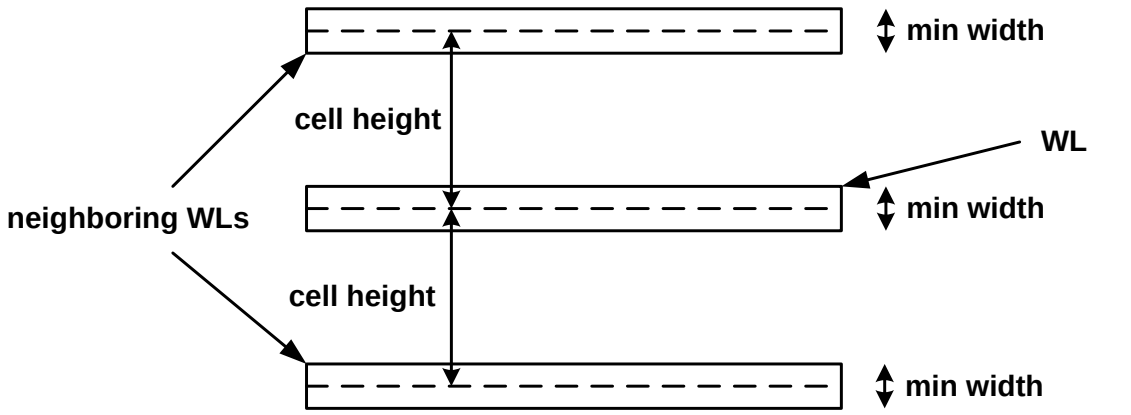
c) Draw a stick diagram of the gate you designed for part b) - you should minimize the diffusion breaks and use a single piece of poly for each input.

d) Now resize the gate to match the worst-case pull-up and pull-down resistances using the velocity saturated model. What is the LE from the B input?

e) Use SPICE to extract the LE from the B input for the gate with the sizing from part d). How does this compare with the result predicted from part d)?

PROBLEM 2: WL Wire for 256x128 SRAM

In this problem we will be looking at a wordline (WL) wire for a 256x128 SRAM array. You should assume that the WL wire is implemented in M2 (which has a minimum width of 0.14μm, R_w = 0.075 Ω/□) and is running over active. You can also assume that there are no higher metal layers running above it. There are other wordlines above and below this worldline, spaced one cell height away (center to center). To calculate the capacitance of this wire, you should use tables 4-2 and 4-3 from the book. You should assume that the cell width is 1.5μm, the cell height is 1μm, that the access device is 120nm wide (which is the minimum width in this technology), and that C_G = 1.6fF/μm.



a) What is the total capacitance of the WL due to the WL wires only (i.e. not including the C_G of the access devices)?

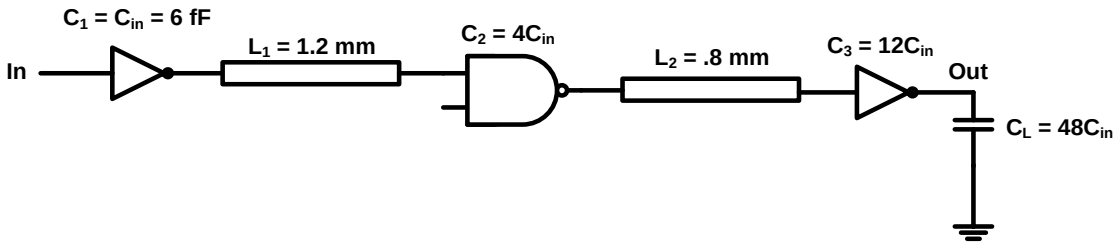
b) What is the total resistance (from the left side of the SRAM to the right side) of the WL wire?

c) Now including the capacitance of the access devices, what is the total RC delay of the WL wire?

d) How much energy is pulled out of the power supply to charge/discharge the wordlines every time the 256x128 SRAM is read?

Problem 3: Logic Chains and Wires

For this problem, use the following parameters for the wire: R_w = 0.075 Ω/□, W = 0.2 μm, and C_w = 0.2 fF/μm (this number includes the effects of both parallel plate and fringe capacitance). For the gates, you should assume that V_{dd} = 1.2V, and for the transistors within the gates, you should assume that C_g = 2 fF/μm, C_d = 1.6 fF/μm, R_{nmos} = 10 kΩ/□, and R_{pmos} = 20 kΩ/□. You should assume that the transistors in the gates are long channel for the purposes of calculating logical effort and sizing. The gates are sized as shown, where C_{in} = 6 fF.



a) Draw an RC model for the above circuit and express the delay from In to Out in terms of L_1, L_2, transistor, and wire parameters. You should include slope effect –

in other words, you can approximate the Elmore delay as being equal to just RC (instead of ln(2)*RC). You can assume that transistors associated with the critical inputs of complex gates are placed as close to the output as possible.

b) Using the expression from part a), what is the total delay of this chain?

c) Now, let's reorganize this chain in order to reduce the total delay. Assuming that the total length of the wires is constant (i.e., $L_1 + L_2 = 2$ mm), what values of L_1 and L_2 give us the optimal delay for the chain? Assume that the size and order of the gates are fixed, and that this path remains critical regardless of how L_1, L_2 change. Using these optimal values of L_1, L_2, what is the optimal delay of the chain under these conditions?