UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

Elad Alon **Homework #8** **EECS141**

Due Tuesday, Nov. 20th @ Dropbox outside 125 Cory

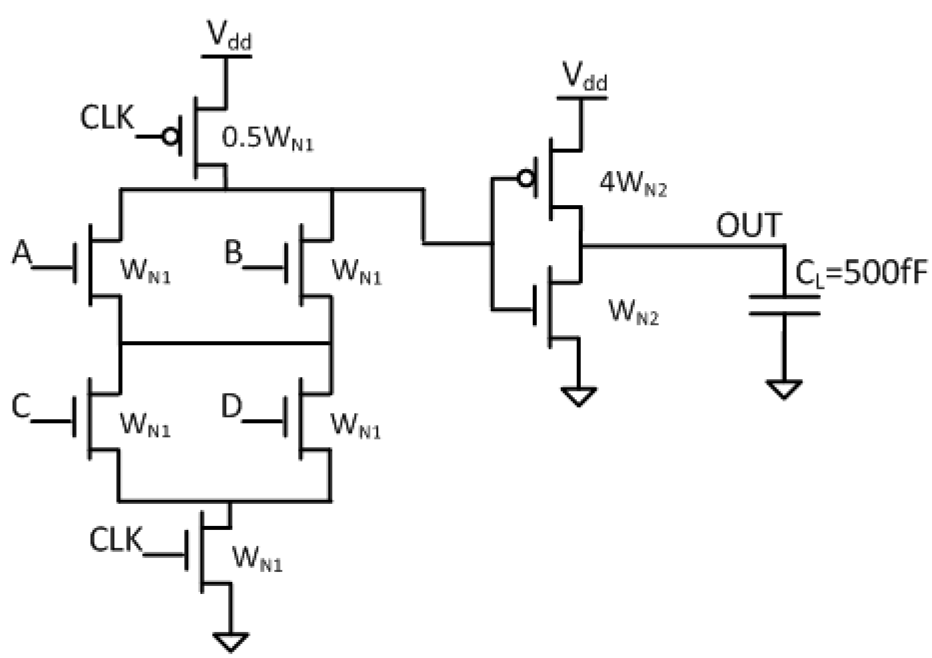
PROBLEM 1: DOMINO LOGIC AND CHARGE SHARING

a) Implement the logic shown below as a single complex, dynamic gate (with four inputs) with a static inverter at the output. You should arrange the dynamic gate such that the worst case drop in its output voltage due to charge sharing is minimized.

$$Out = A(B + C)D$$

b) What pattern of the inputs A, B, C and D results in the worst-case drop in the dynamic gate's output voltage due to charge sharing? Assuming that V_{DD} = 1.2V, C_G = 2fF/μm, C_D = 1.5fF/μm, that the NMOS pull-down network in the dynamic gate is sized to have the same worst-case resistance (with long-channel transistors) as the pre-charge PMOS transistor, and that the input capacitance of the inverter is 4 times that of the dynamic gate, what is this worst-case dynamic gate output voltage?

PROBLEM 2: DOMINO SIZING AND DELAY



Consider the domino circuit above. Assume long-channel transistors, C_L = 500fF, C_{in} = 4fF, C_G = 2fF/μm, C_D = 1.5fF/μm, and that input signal A is the last one to arrive.

a) Find the logical effort of each stage in the critical path for the evaluation edge (rising edge of Out).

b) Find WN1 and WN2 to give minimal delay.

c) Estimate the delay of the critical path in F04. Include the worst-case parasitic delay terms. Recall that 1FO4 is equal to $(4+\gamma)t_{inv}$.

d) From the standpoint of minimum delay, is this the optimum number of stages? If not, how many stages would you use to minimize the delay?