UNIVERSITY OF CALIFORNIA, BERKELEY
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Elad Alon **Homework #9 (Optional)** **EECS141**

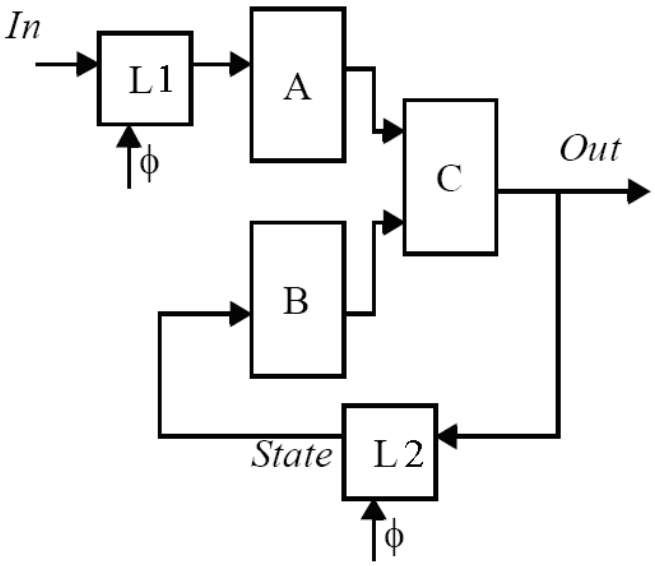
PROBLEM 1: LOGIC STYLES

Problems 3)b) and 3)c) from the EE141 Fall07 Midterm #2 (available on the web).

PROBLEM 2: FLIP-FLOP TIMING

Problem #4 from the EE141 Fall08 Final (available on the web).

PROBLEM 3: "PULSED" LATCH TIMING



Consider the simple state machine shown above. A, B, and C represent combinational logic blocks with the following properties:

$t_{logic,minA}$ = 200 ps; $t_{logic,maxA}$ = 1 ns;
$t_{logic,minB}$ = 300 ps; $t_{logic,maxB}$ = 2 ns;
$t_{logic,minC}$ = 100 ps; $t_{logic,maxC}$ = 0.5 ns;

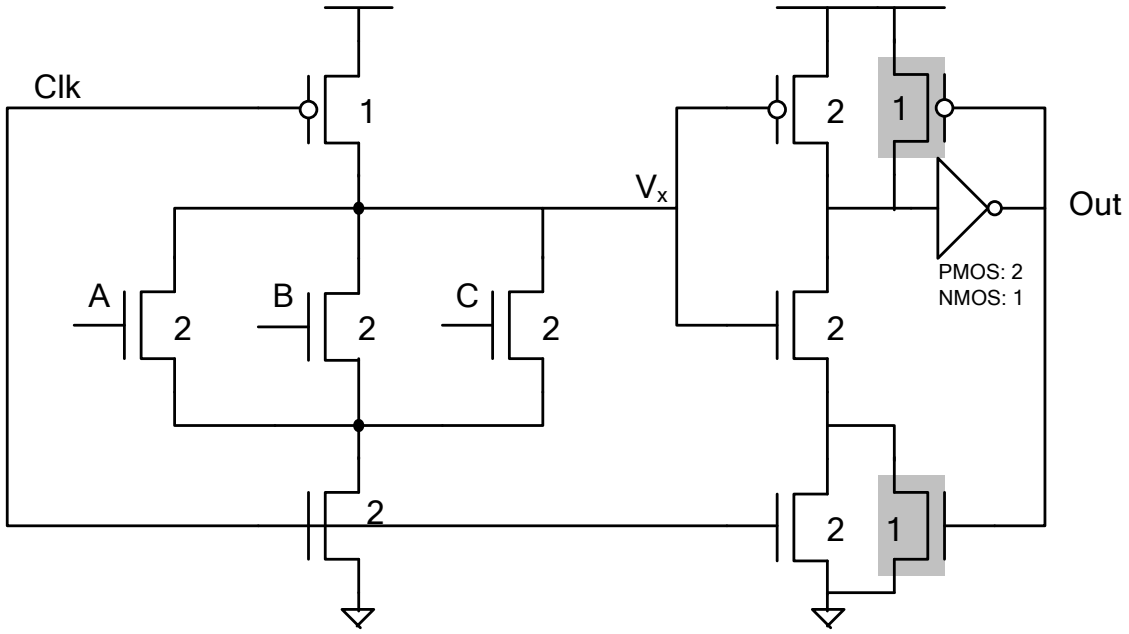
The L-units represent **positive latches** clocked by ϕ (i.e., the latches are transparent when ϕ is high). These latches have a setup time of 150 ps and a $t_{d\text{-}q}$ delay of 250 ps (when the latch is transparent). The clock to output delay $t_{clk\text{-}q}$ is 100 ps, and t_{hold} is 100 ps. The clock ϕ has a period T_{clk} and is high for a duration of T_{on} – in other words, the duty cycle of the clock is T_{on}/T_{clk}.

a) Determine the conditions on the clock necessary to avoid the occurrence of hold-time violations.

b) Determine the absolute minimum clock period for this circuit to work correctly as well as the maximum duty cycle.

c) Suppose that due to some sloppy clock-network routing, the clock signal at L1 arrives 100ps earlier than the clock signal at L2. Calculate the absolute minimum clock period for this circuit to work properly as well as the maximum duty cycle.

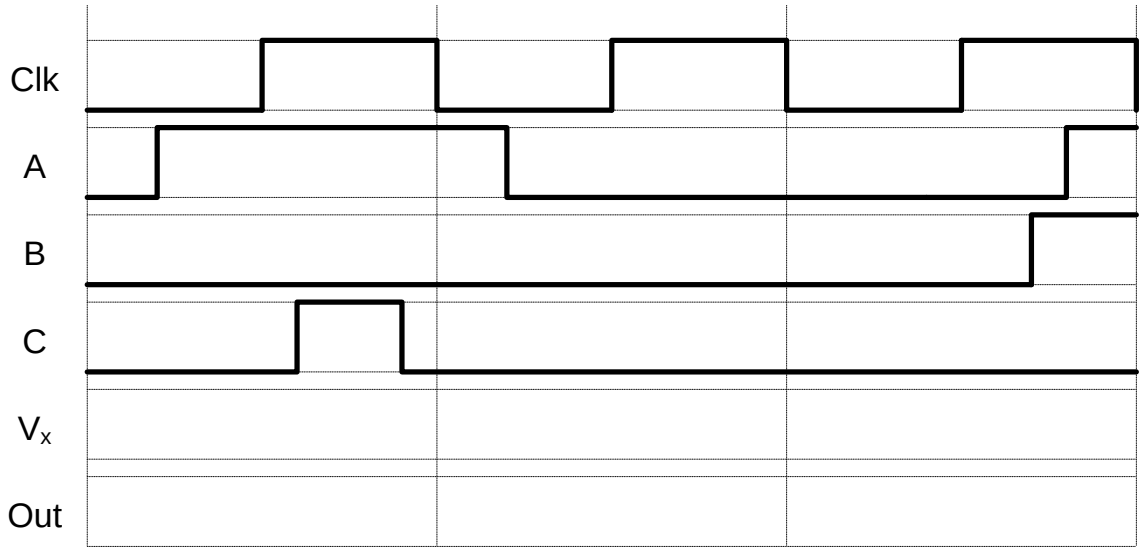
PROBLEM 4: LIMITED SWITCH DYNAMIC LOGIC



The circuit above (with relative transistor sizes annotated) is a Limited Switch Dynamic Logic (LSDL) NOR3 gate, which is essentially a dynamic gate followed by a latch.

a) What purpose are the shaded transistors serving?

b) Assuming no propagation delay, complete the following ideal timing diagram.



c) Calculate the t_{setup} of this gate in terms of t_{inv}. In other words, how long before the falling edge of the clock do the inputs have to be stable to ensure that the correct value is latched at the output? You can assume that $\gamma=1$.

d) Assuming that A=B=C=1, compare the activity factor at node *Out* to the activity factor at node V_x (which would be the output of a standard dynamic logic gate). What can you infer about the dynamic power consumption of static gates being driven by this LSDL gate compared to gates driven by domino logic?