What is this class all about?

- Introduction to digital integrated circuit design engineering
  - Will describe models and key concepts needed to be a good digital IC designer
- Models allow us to reason about circuit behavior
  - Allow analysis and optimization of the circuit's performance, power, cost, etc.
  - Understanding circuit behavior is key to making sure it will actually work
- Teach you how to make sure your circuit works
  - Do you want your transistor to be the one that screws up a 1 billion transistor chip?

What will you learn?

- Understanding, designing, and optimizing digital circuits for various quality metrics:
  - Performance (speed)
  - Power dissipation
  - Cost
  - Reliability

Detailed Topics

- CMOS devices and manufacturing technology
- CMOS gates
- Memories
- Propagation delay, noise margins, power
- Combinational and sequential circuits
- Interconnect
- Timing and clocking
- Arithmetic building blocks
- Design methodologies

Practical Information

- Instructor
  - Prof. Elad Alon
  - 519 Cory Hall, 642-0237, elad@eecs
  - Office hours: Tu. 3:30-4:30pm, Thurs. 2:30-3:30pm
- TAs:
  - Alberto Puggelli, puggelli@eecs (OH: Wed. 4-5pm)
  - Bonjern Yang, byang@eecs (OH: Wed. 3-4pm)
- Web page:
  - http://bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141_f12/

Discussions and Labs

- Discussion sessions
  - F 2-3pm (Bonjern)
  - M 5-6pm (Alberto)
  - Same material in all sessions!
- Labs (125 Cory)
  - M 3-6pm (Bonjern)
  - Tu 3-6pm (Alberto)
  - Machines to left of double doors, with larger monitors
- Please choose one lab session and stick with it!
Your EECS141 Week

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* Discussion sections will cover identical material

Grading Policy

- Homeworks: 12%
- Labs: 8%
- Projects: 20%
- Midterms: 30%
- Final: 30%

Class Organization

- 9 Assignments
- One design project (with a few phases)
- Labs: 5 software
- 2 midterms, 1 final
  - Midterm 1: Thurs., October 4, evening (TBD)
  - Midterm 2: Thurs., November 1, evening (TBD)
  - Final: Wed., December 12, 8-11am

Class Material

- Class notes: Web page
- Lab Reader: Web page
- Check web page for the availability of tools

Some Important Announcements

- Please use piazza for asking questions (more later)
- Can work together on homework
  - But you must turn in your own solution
- Lab reports due 1 week after the lab session
  - Lab rules: http://california.eecs.berkeley.edu/iesg/labs/labinfo/labrules.asp
- Project is done in pairs
- No late assignments
  - Solutions available shortly after due date/time
- Don’t even think about cheating!

The Web Site

http://bwrc.eecs.berkeley.edu/icdesign/ee141_f10

- Class and lecture notes
- Assignments and solutions
- Lab and project information
- Exams
- Many other goodies …

Print only what you need: Save a tree!
**The Web Site #2**

- All announcements made at: [https://piazza.com/berkeley/fall2012/ee141](https://piazza.com/berkeley/fall2012/ee141)
- Be sure to enroll!
- Piazza will also be the main forum for posting and answering questions
  - Please post your questions there to minimize response time
  - Also, check that your question hasn’t been answered already

**Introduction**

  - What made Digital IC design what it is today
  - Why is designing digital ICs different today than it was before?
  - Will it change in the future?

**Software**

- Cadence
  - Widely used in industry
  - Online tutorials and documentation
- HSPICE for simulation

**The First Computer**

- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470

**Getting Started**

- Assignment 1: Getting SPICE to work – see web-page
- Due next Thursday, August 30, 5pm
- NO discussion sessions or labs this week.
- First discussion sessions in Week 2
- First software lab in Week 3

**ENIAC - The First Electronic Computer (1946)**
The Transistor Revolution

First transistor
Bell Labs, 1948

Intel Pentium 4 Microprocessor

Intel, 2005.
125,000,000 transistors
(112mm²)
3.8 GHz operation
(90nm CMOS technology)

The First Integrated Circuits

Bipolar logic
1960's

Intel Xeon (E7-8800)

Intel, 2011.
2,600,000,000 transistors
(513mm²)
2.4 GHz operation
(32nm CMOS technology)

Intel 4004 Microprocessor

2,300 transistors (12mm²)
740 kHz operation
(10µm PMOS technology)

Still Happening - Intel Test-Chip (2009)

22nm
364 MByte SRAM
>2.91 billion transistors
Moore’s Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months.
Power Dissipation Data

Has been > doubling every 2 years

Has to stay ~constant

Power Trends in Intel's Microprocessors

Cause: Power Density

Power density too high for cost-effective cooling

Challenges in Digital Design

Not enough cooling...

Production Trends

Complexity outpaces design productivity

Not Only Microprocessors

Digital Cellular Market (Phones Shipped)

Cells

Power Management

Small Signal RF

RF (data from Texas Instruments)

Challenges in Digital Design

"Microscopic Problems"
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

...and There's a Lot of Them!

Cell Phone

Units

48M  86M  162M  260M  435M

(data from Texas Instruments)

Source: Sematech

Complexity outpaces design productivity

Productivity Trends

Courtesy, ITRS Roadmap
**Why Scaling?**

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But ...
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years...
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

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**Design Abstraction Levels**

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**Next Lecture**

- Introduce basics of integrated circuit manufacturing and cost