Announcements

- Homework #5 due Thursday
  - Homework #6 out next week

- Midterm #1 Thurs. Oct. 4th, 6:30-8:00pm
  - Location TBD
  - Exam is open notes, book, calculators, etc.
  - Midterm review session next week

- Elad out of town this Thurs. and Fri.
  - Thurs. lecture will be taped ahead tomorrow
    (Wed.) 11am-12:30pm – location TBD
Class Material

- Last lecture
  - MOS Transistor Model
- Today’s lecture
  - Using the MOS Model: Inverter VTC
- Reading (5.1-5.3)

CMOS Inverter VTC
The CMOS Inverter

\[ V = V_{DD} - V_{out} \]

\[ W_p = \beta W_n \]

PMOS Load Lines

- For DC VTC, \( I_{Dn} = I_{DP} \)
  - Graphically, looking for intersections of NMOS and PMOS IV characteristics

- To put IV curves on the same plot, PMOS IV is “flipped” since \( |V_{DSP}| = V_{DD} - V_{out} \)
  - Also, \( |V_{GSP}| = V_{dd} - V_{in} \)

\[ I_{Dn} = I_{DP} \]

\[ V_{in} = V_{out} \]

\[ V_{in} = 2.5 \]

\[ V_{in} = 1.5 \]

\[ V_{in} = 0 \]

\[ V_{in} = 1.5 \]
Note on Transistor IV Problems

- “Guess and Check”
  - Guess region(s) of operation
  - Check consistency

CMOS Inverter VTC
Switching Threshold as a Function of Transistor Ratio

\[ I_{d_n}(V_M) = I_{d_p}(V_M) \]

Solving for \( V_M \) yields:

\[ V_M = \frac{V_{th}^* + r(V_{DD} - V_{th}^*)}{1 + r} \]

with \( r = \frac{k_n \cdot V_{th}^*}{k_p \cdot V_{th}^*} = \frac{W_p \cdot V_{th}}{W_n \cdot V_{th}} \).
Determining $V_{IH}$ and $V_{IL}$

$V_{IH} - V_{IL} = \frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$

$V_{IH} = V_{M} - \frac{V_{M}}{g}$

$V_{IL} = V_{M} + \frac{V_{DD} - V_{M}}{g}$

$NM_{H} = V_{DD} - V_{IH}$

$NM_{L} = V_{IL}$

Gain as a function of VDD
**Impact of Sizing**

![Graph](attachment:image.png)

- **Wider PMOS**
- **Wider NMOS**
- **Symmetrical**

**Process Variations**

Not all transistors are alike

Impacts parameters such as reliability and performance

Define process corners: SS, FF, SF, FS
**Impact of Process Variations**

- **Fast PMOS**
- **Slow NMOS**
- **Slow PMOS**
- **Fast NMOS**
- **Nominal**