Announcements

- Homework #5 due Thursday
  - Homework #6 out next week
- Midterm #1 Thurs. Oct. 4th, 6:30-8:00pm
  - Location TBD
  - Exam is open notes, book, calculators, etc.
  - Midterm review session next week
- Elad out of town this Thurs. and Fri.
  - Thurs. lecture will be taped ahead tomorrow (Wed.) 11am-12:30pm – location TBD

Class Material

- Last lecture
  - MOS Transistor Model
- Today’s lecture
  - Using the MOS Model: Inverter VTC
- Reading (5.1-5.3)

PMOS Load Lines

- For DC VTC, $I_{DP} = I_{DN}$
  - Graphically, looking for intersections of NMOS and PMOS IV characteristics
- To put IV curves on the same plot, PMOS IV is “flipped” since $|V_{DSS}| = V_{DD} - V_{out}$
  - Also, $|V_{DSS}| = V_{DD} - V_{out}$

The CMOS Inverter

- $W_p = \beta W_n$
- $V_{DD}$
- $V_{IN}$
- $V_{OUT}$
- $W_n$
- $V_{DSn}$
- $|IDn| = |IDp|$
Note on Transistor IV Problems

- "Guess and Check"
  - Guess region(s) of operation
  - Check consistency

CMOS Inverter VTC

Switching Threshold as a Function of Transistor Ratio

Determining $V_{IH}$ and $V_{IL}$

Switching Threshold as a Function of Transistor Ratio

Gain as a function of VDD
Impact of Sizing

Process Variations
Not all transistors are alike
Impacts parameters such as reliability and performance
Define process corners: SS, FF, SF, FS

Impact of Process Variations