EE141-Fall 2012
Digital Integrated Circuits

Lecture 12
CMOS Delay and Power Models

Announcements

- Midterm #1 Thurs., 6:30-8:00pm, 141 McCone
  - Be sure to arrive on time

- Midterm review session today, 6pm, 550 Cory

- Lecture will be “taped-ahead” for this Thurs..

- Homework #6 out this Thurs., due next Thurs.
Class Material

- Last lecture
  - MOS Capacitance, delay
- Today’s lecture
  - Improved CMOS Delay and Power Models
- Reading (5.1-5.3, 5.4.2)

Propagation Delay
**Transient Response**

\[ t_{pHL} = \ln(2) C_L R_{eqn} \]
\[ t_{PLH} = \ln(2) C_L R_{eqp} \]

\[ R_{eq} = \frac{1}{2 \ln(2)} \frac{1}{1 + 2V_{DD} I_{DSAT}} \]

---

**Step Inputs?**

- Derived RC model assuming input was a step
  - But input is not a step
  - Transistor turns on gradually

- Let’s look at gate switching more carefully
  - Use our models to understand the effect of input slope
**Input Slope Dependence**

- One way to analyze slope effect
  - Plug non-linear IV into diff. equation and solve...
- Simpler, approximate solution:
  - Use $V_T^*$ model

\[ I_{out} = C_L \frac{dV_{out}}{dt} = I_{NMOS} - I_{PMOS} \]

**Slope Analysis**

- For falling edge at output:
  - For reasonable inputs, can ignore $I_{PMOS}$
  - Either $V_{ds}$ is very small, or $V_{gs}$ is very small

- So, output current ramp starts when $V_{in} = V_T^*$
  - Could evaluate the integral implied by slide 7
  - Learn more by using an intuitive, graphical approach
Slope Effect
Result Summary

- For reasonable input slopes:

\[ t_{p,\text{ramp}} = t_{p,\text{step}} + \frac{V_T^*}{V_{DD}} \cdot t_{p,\text{in}} \]

- For \( t_{p,\text{avg}} \), \( V_T^* \) is \( (V_{TN^*} + V_{TP^*})/2 \)
  - \( V_T^*/V_{DD} \) typically \( \sim 1/3 \) at nominal supply

Model vs. Spice Data

- For reasonable input slope
  - Model matches Spice very well

- Model breaks with very large \( t_r \)
  - Input looks “DC” – traces out VTC
  - Have other problems here anyways
    - Short-circuit current
Implications

- Delay of an inverter after a long chain:
CMOS Power Dissipation

Where Does Power Go in CMOS?

- Switching power
  - Charging/discharging capacitors

- Leakage power
  - Transistors are imperfect switches

- Short-circuit power
  - Both pull-up and pull-down on during transition

- Static currents
  - Biasing currents, in e.g. analog, memory
Dynamic Power Consumption

- One half of the energy from the supply is consumed in the pull-up network, one half is stored on $C_L$.
- Energy from $C_L$ is dumped during the $1 \rightarrow 0$ transition.

\[ E_{0\rightarrow1} = C_L V_{DD}^2 \]
\[ E_R = \frac{1}{2} C_L V_{DD}^2 \]
\[ E_C = \frac{1}{2} C_L V_{DD}^2 \]

Circuits with Reduced Swing

\[ E_{0\rightarrow1} = \]

\[ V_{DD} \]
\[ V_{DD} - \Delta V \]
Dynamic Power Consumption

Power = Energy/transition • (Transition rate/2)
= Energy/transition • (Rising transition rate)

= $C_L V_{DD}^2 \cdot f_{0\rightarrow1}$
= $C_L V_{DD}^2 \cdot f \cdot P_{0\rightarrow1}$
= $C_{\text{switched}} V_{DD}^2 \cdot f$

- Power dissipation is data dependent – depends on the switching probability
- Switched capacitance $C_{\text{switched}} = C_L \cdot P_{0\rightarrow1}$

Transition Activity and Power

- Energy consumed in $N$ cycles, $E_N$:

$$E_N = C_L \cdot V_{DD}^2 \cdot n_{0\rightarrow1}$$

$n_{0\rightarrow1}$ – number of $0\rightarrow1$ transitions in $N$ cycles

$$P_{\text{avg}} = \lim_{N\rightarrow\infty} \frac{E_N}{N} \cdot f = \left( \lim_{N\rightarrow\infty} \frac{n_{0\rightarrow1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\rightarrow1} = \lim_{N\rightarrow\infty} \frac{n_{0\rightarrow1}}{N}$$

$$P_{\text{avg}} = \alpha_{0\rightarrow1} \cdot C_L \cdot V_{DD}^2 \cdot f$$
**Short Circuit Current**

- Short circuit current usually well controlled

![Short Circuit Current Diagram](image)

**Transistor Leakage**

- Transistors that are supposed to be off actually leak

![Transistor Leakage Diagram](image)
**Diode Leakage**

\[
\text{Reverse Leakage Current}
\]

\[
I_{DL} = J_S \times A
\]

- \(J_S = 10-100 \text{ pA/\mu m}^2\) at 25 deg C for 0.25\(\mu\)m CMOS
- \(J_S\) doubles for every 9 deg C!
- Much smaller than transistor leakage in deep submicron

---

**Transistor Leakage**

\[
V_{DS} = 1.2V
\]

Drain leakage current is exponential with \(V_{GS} - V_T\)
**Sub-Threshold Conduction**

Inverse Subthreshold Slope:

\[ I_D \sim I_0 e^{\frac{q(V_{GS} - V_T)}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}} \]

\[ S^{-1} \text{ is } \Delta V_{GS} \text{ for } I_{D2}/I_{D1} = 10 \]

\[ S^{-1} = n \left( \frac{kT}{q} \right) \ln(10) \]

Typical values for \( S^{-1} \): 
60 .. 100 mV/decade

**Transistor Leakage vs. \( V_{DS} \)**

Two effects:
- diffusion current (like a bipolar transistor)
- exponential increase with \( V_{DS} \) (\( \eta \): DIBL)
Threshold Variations

Threshold as a function of length (for low $V_{DS}$)

Drain-induced barrier lowering (DIBL) (for short $L$)

Power Summary
Next Lecture

- CMOS Logic Review