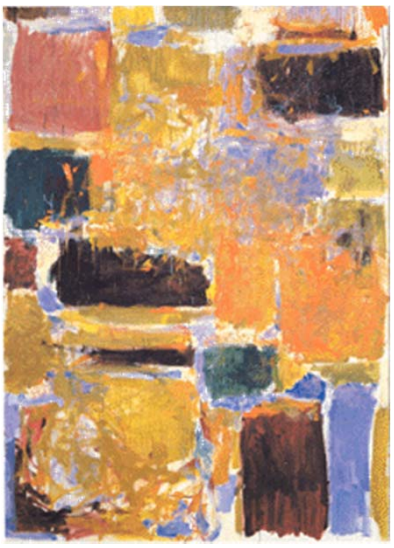


EE141-Fall 2012 Digital Integrated Circuits

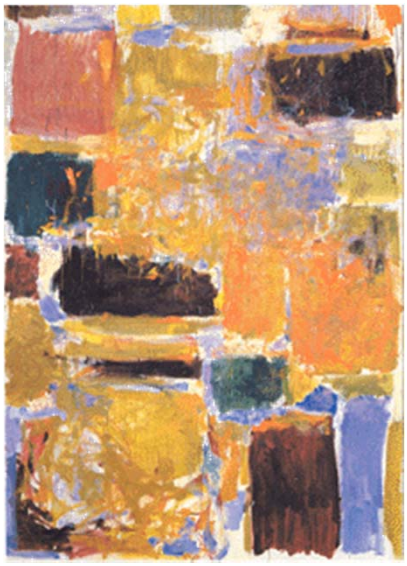
Lecture 13
CMOS Logic Review

Announcements

- Midterm tonight 6:30pm sharp
- Homework #6 out tonight, due next Thurs.
- Reminder:
  - Project coming up in 2 weeks – find a partner

Class Material

- Last lecture
  - CMOS Delay and Power Models
- Today's lecture
  - CMOS Logic Review
- Reading (6)

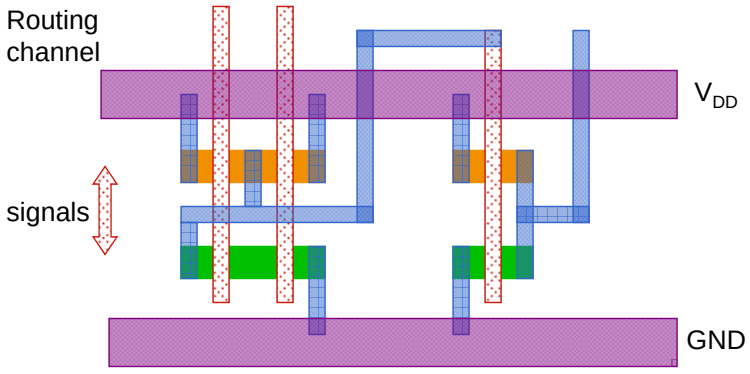


CMOS Logic Review

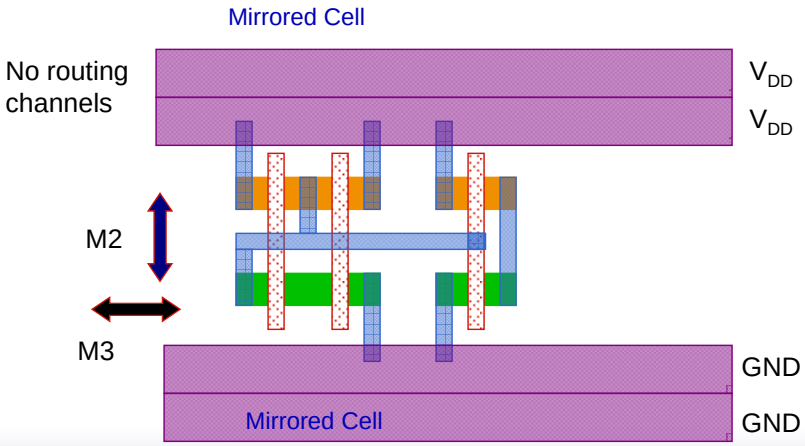
Cell Design

- Standard Cells
  - General purpose logic
  - Used to synthesize RTL/HDL
  - Same height, varying width
- Datapath Cells
  - For regular, structured designs (arithmetic)
  - Includes some wiring in the cell

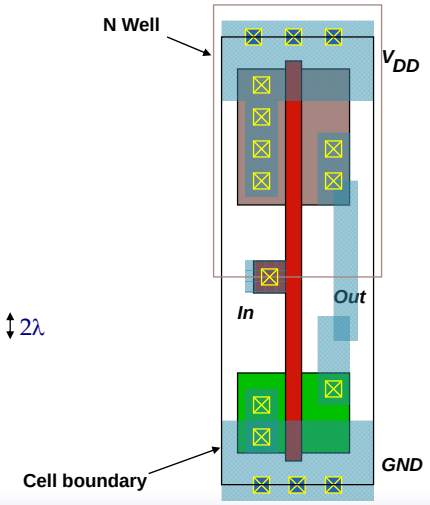
Standard Cell Layout Methodology – 1980s



Standard Cell Layout Methodology – 1990s - Today



Standard Cells



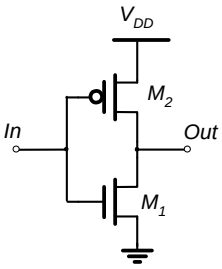
Cell height 12 metal tracks
Metal track is approx. 3λ + 3λ
Pitch =
repetitive distance between objects

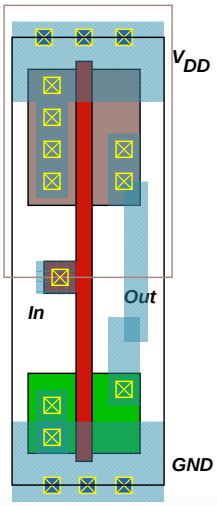
Cell height is "12 Mn pitch"

Rails ~10λ

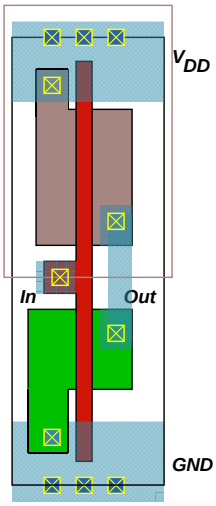
Standard Cells

With minimal diffusion routing





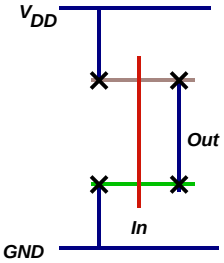
With silicided diffusion



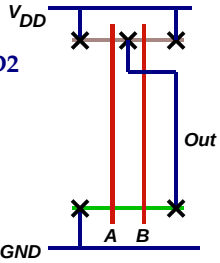
Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

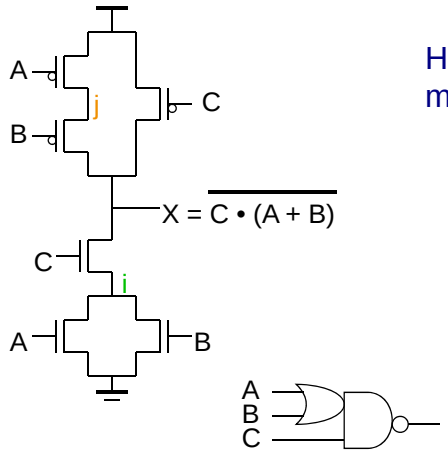
Inverter



NAND2

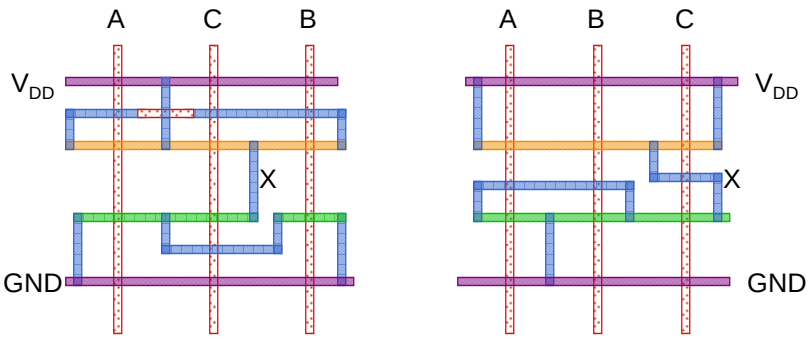


Stick Diagrams



How to lay this gate out to minimize area?

Two Versions of $\overline{C \bullet (A + B)}$



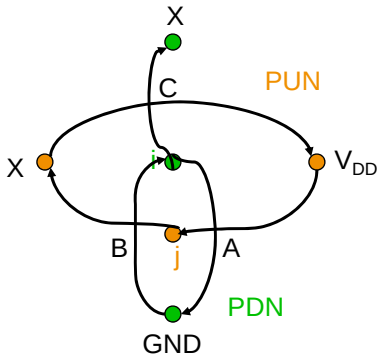
Consistent Euler Path

A B C

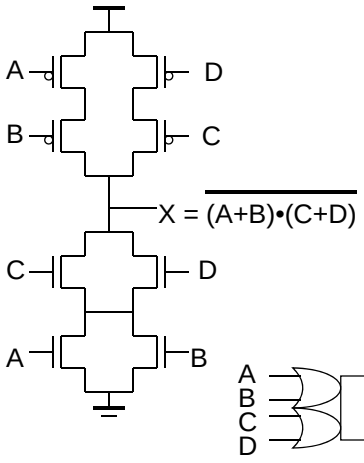
Has PDN and PUP

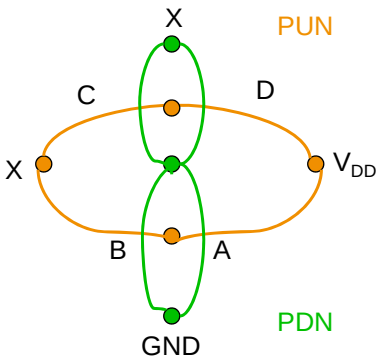
B C A

Has PUP, but no PDN

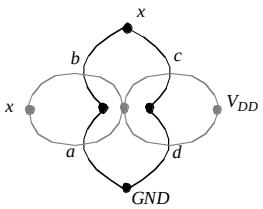


OAI22 Logic Graph

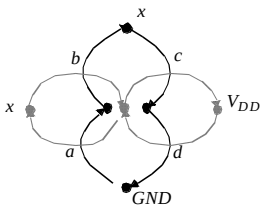




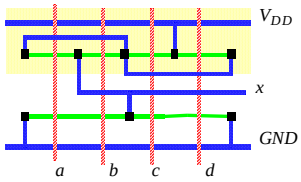
Example: x = ab+cd



(a) Logic graphs for $\overline{(ab+cd)}$



(b) Euler Paths {*a b c d*}

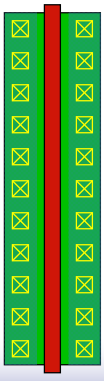


(c) stick diagram for ordering {a *b c d*}

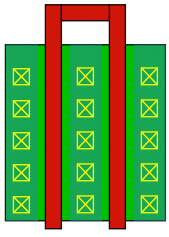
Multi-Fingered Transistors

How can you fit wide transistors into a fixed height?

One finger



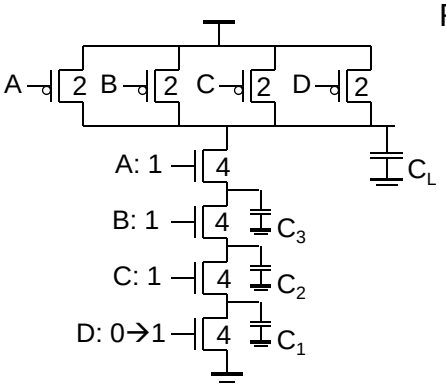
Two fingers (folded)



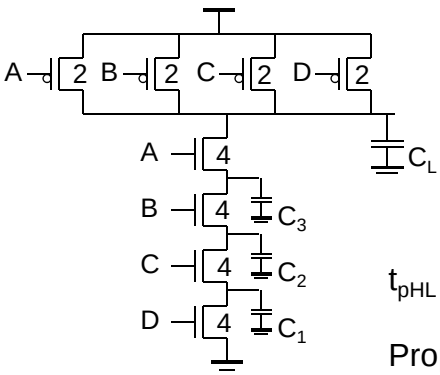
Less diffusion capacitance

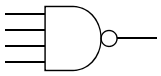
Fan-In Considerations

RC model:



Fan-In Considerations



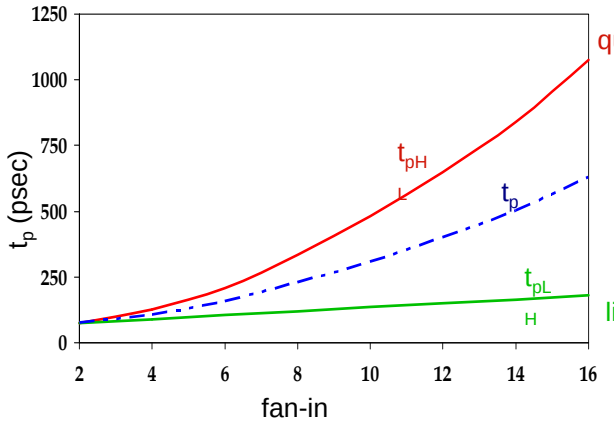


Distributed RC model (Elmore delay)

$t_{pHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

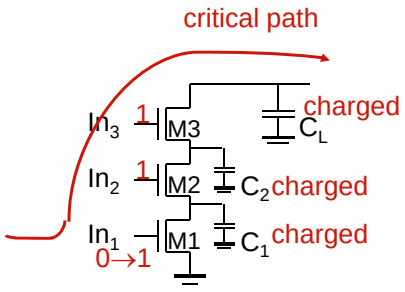
t_p as a Function of Fan-In



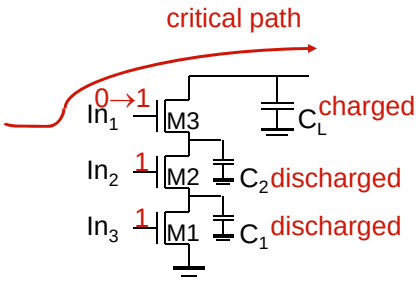
Gates with a fan-in greater than 4 should be avoided.

Reducing Parasitic Delay (1)

- Transistor ordering



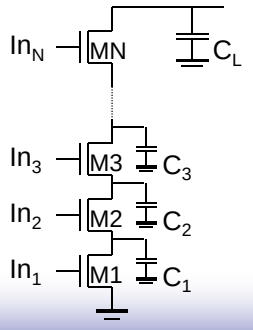
delay determined by time to discharge C_L, C_1 and C_2



delay determined by time to discharge C_L

Reducing Parasitic Delay (2)

- Transistor sizing
  - as long as fan-out capacitance dominates
- Progressive sizing



Distributed RC line

M1 > M2 > M3 > … > MN
(the FET closest to the output is the smallest)

Can reduce delay by more than 20%;
Be careful: input loading, junction caps, decreasing gains as technology shrinks

Reducing Delay (3)

- Reducing the voltage swing

$$t_{pHL} = 0.5\,(C_L\,V_{DD}) / I_{DSATn}$$

$$= 0.5\,(C_L\,V_{swing}) / I_{DSATn}$$

  - linear reduction in delay
  - also reduces power consumption
- But the following gate is slower!
- Or requires use of “sense amplifiers” on the receiving end to restore the signal level (memory design)

LE in Modern Processes

LE in Modern Processes

Next Lecture

- Wires