EE141-Fall 2012 Digital Integrated Circuits

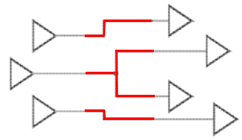
Lecture 14
Wires

Announcements

- Homework #6 due this Thurs.
  - Homework #7 out this Thurs.
- Project #1 out Oct. 18th
  - Find a partner

Wires

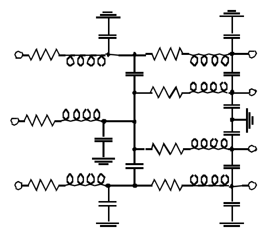
The Wire



Schematic

Physical

Wire Models

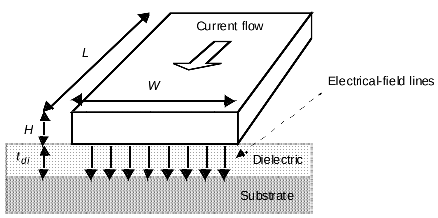


Impact of Interconnect Parasitics

- Interconnect and its parasitics can affect all of the metrics we care about
  - Cost, reliability, performance, power consumption
- Parasitics associated with interconnect:
  - Capacitance
  - Resistance
  - Inductance

INTERCONNECT

Capacitance: The Parallel Plate Model



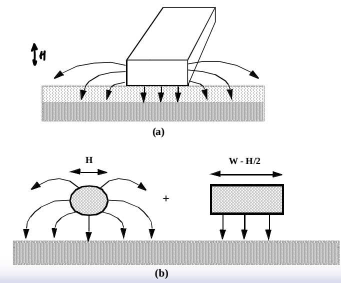
$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Permittivity

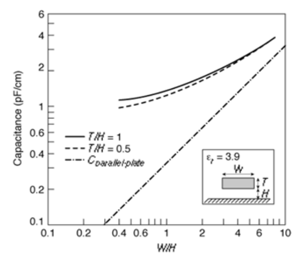
Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringing Capacitance

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

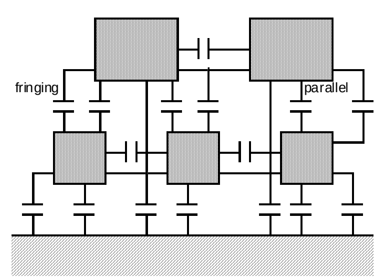


Fringing versus Parallel Plate

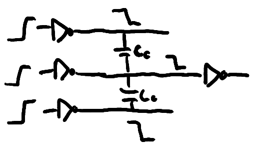


(from [Bakoglu89])

Interwire Capacitance

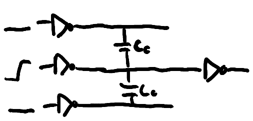


Coupling Capacitance and Delay



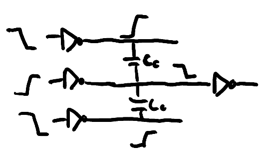
$C_{c,eff} =$

Coupling Capacitance and Delay



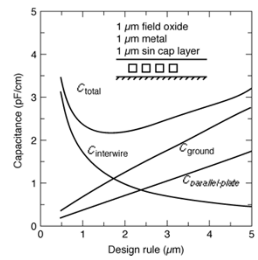
$C_{c,eff} =$

Coupling Capacitance and Delay



$C_{c,eff} =$

Impact of Interwire Capacitance



(from [Bakoglu89])

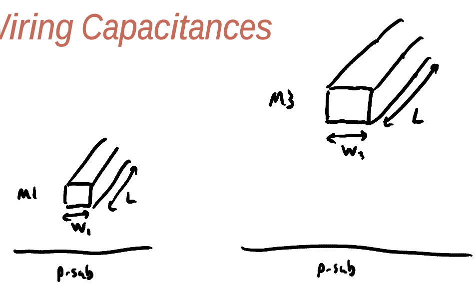
Wiring Capacitances (0.25 μm CMOS)

Bottom plate

Top plate

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88	aF/μm²					
	54	aF/μm					
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Wiring Capacitances

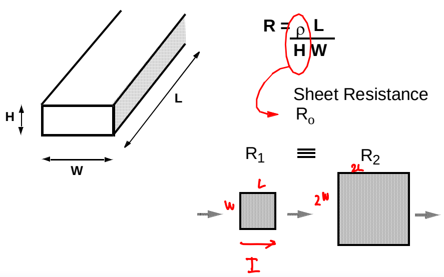


$C = C_{pp} \cdot W \cdot L + 2 C_{fringe} L$

INTERCONNECT

Resistance

Wire Resistance



Dealing with Resistance

- Better materials:

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

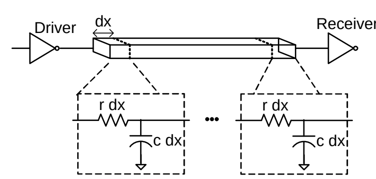
- More layers:

Example Numbers

Material	Sheet Resistance (Ω/□)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

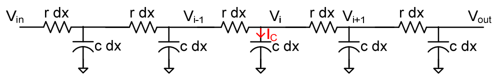
Interconnect Modeling

The Distributed RC-line



- Analysis method:
  - Break the wire up into segments of length dx
  - Each segment has resistance (r dx) and capacitance (c dx)

The Distributed RC-line



$$I_C = c\Delta L \frac{\partial V}{\partial t} = \frac{(V_{i-1} - V_i) - (V_i - V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2} rc}$$

Wire Model

Model the wire with N equal-length segments:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

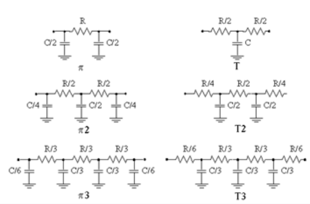
For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



Wire Delay Example

Next Lecture

- SRAM Circuit Design