Announcements

- Homework #6 due today
  - Homework #7 due next Thurs.
  - Project #1 out next Thurs.
SRAM Circuit Design

6-transistor CMOS SRAM Cell

\[ \text{Diagram of 6-transistor CMOS SRAM Cell} \]
**SRAM Column**

- WL0
- WL2
- WL3
- BL
- BL_B

**SRAM Operation**

- **Write**
  - WL
  - BL
  - BL
  - 0
  - 1

- **Hold**
  - WL
  - BL
  - BL
**SRAM Operation**

**Read**

- Q_\_b will get pulled up when WL first goes high
- Reading the cell should not destroy the stored value

\[ I_{D3} = I_{D1} \]

\[ W_{SV} C_{\text{ox}} \left( \frac{V_{DD} - V_{th} - \Delta V}{V_{DD} - V_{th} - \Delta V + \xi_{crit,n} L_{n}} \right)^{2} = \mu_{n} C_{\text{ox}} \frac{W_{1}}{L_{1}} \left( V_{DD} - V_{th} - \frac{\Delta V}{2} \right) \Delta V \]
**CMOS SRAM Analysis (Read)**

![Graph showing voltage rise vs. cell ratio (CR)]

Cell Ratio (CR) vs. Voltage Rise (ΔV)

CR = \( \frac{W_1}{L_1} \)

**CMOS SRAM Analysis (Write)**

![Diagram of CMOS SRAM write operation]

\[
W_4V_{dd}C_m \left( \frac{V_{dd} - V_p}{V_{dd} - V_p + 2 V_t} \right)^2 = \mu_C \frac{W}{L_6} \left( V_{dd} - V_n - V_0 \right) V_Q
\]
**CMOS SRAM Analysis (Write)**

![Graph showing cell voltage vs pull-up ratio](image1)

\[
PR = \frac{(W/L)_4}{(W/L)_6}
\]

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**Read Static Noise Margin**

![Diagram showing read static noise margin](image2)

Obtained by breaking the feedback between the inverters.
Write Static Noise Margin

Alternate Definition for Write Margin

\[ \text{WNM: max. } V_{bi} \text{ where cell still flips} \]
Next Lecture

- Power Revisited