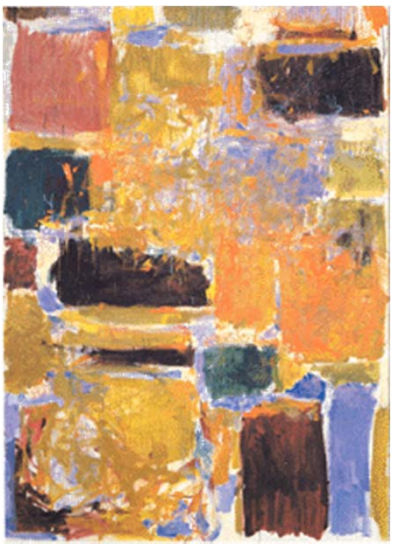


EE141-Fall 2010 Digital Integrated Circuits

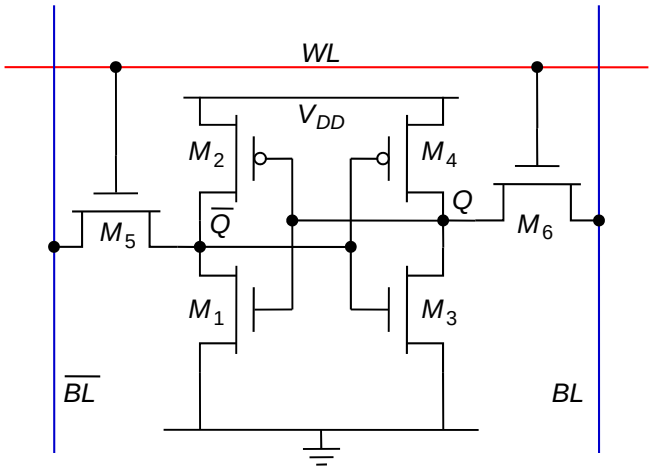
Lecture 15
SRAM Circuit Design

Announcements

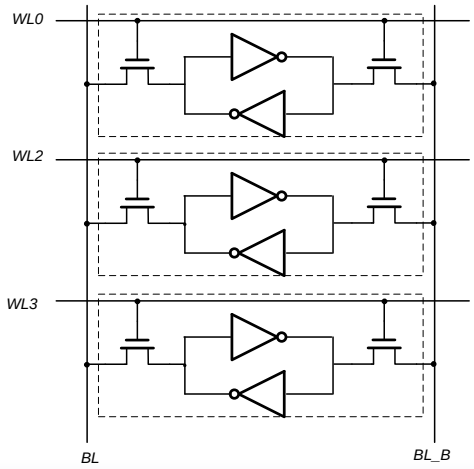
- Homework #6 due today
  - Homework #7 due next Thurs.
  - Project #1 out next Thurs.

SRAM Circuit Design

6-transistor CMOS SRAM Cell

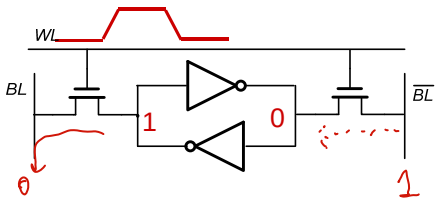


SRAM Column

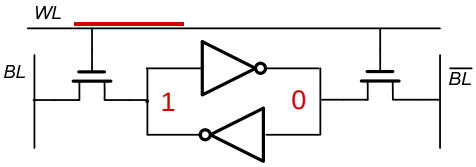


SRAM Operation

Write

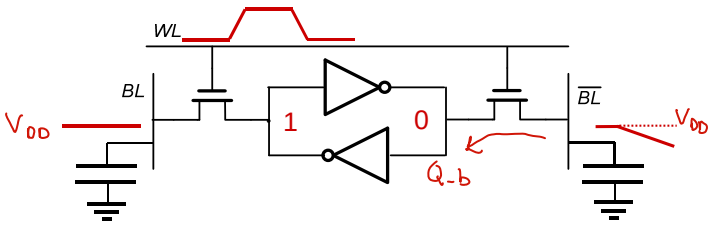


Hold



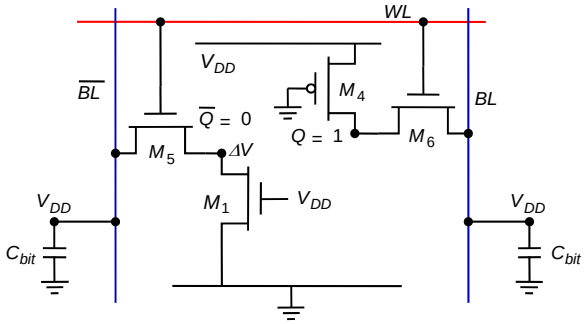
SRAM Operation

Read



- Q_b will get pulled up when WL first goes high
  - Reading the cell should not destroy the stored value

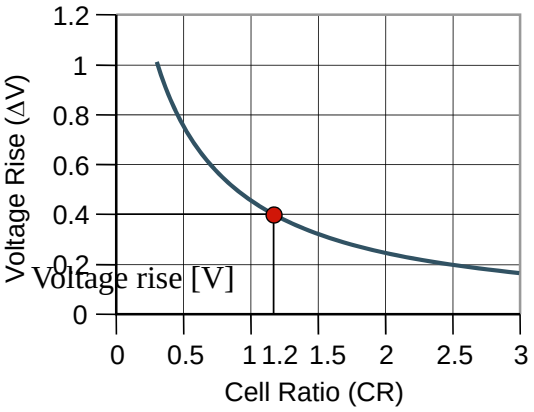
CMOS SRAM Analysis (Read)



$$I_{D5} = I_{D1}$$

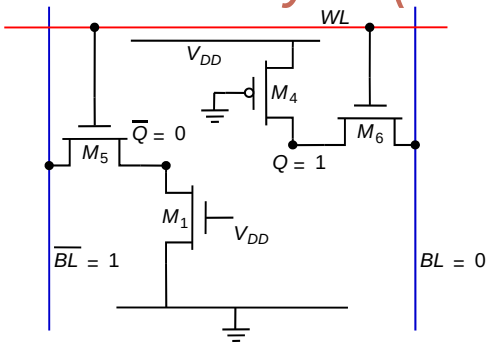
$$W_5 v_{sat} C_{ox} \frac{(V_{DD} - V_{Tn} - \Delta V)^2}{V_{DD} - V_{Tn} - \Delta V + \xi_{crit,n} L_5} = \mu_n C_{ox} \frac{W_1}{L_1}\left(V_{DD} - V_{Tn} - \frac{\Delta V}{2}\right)\Delta V$$

CMOS SRAM Analysis (Read)



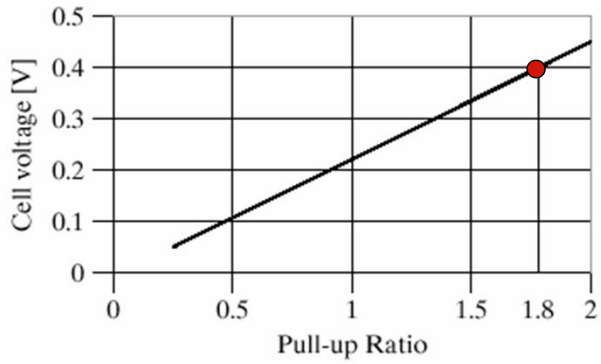
$$CR = \frac{W_1/L_1}{W_5/L_5}$$

CMOS SRAM Analysis (Write)



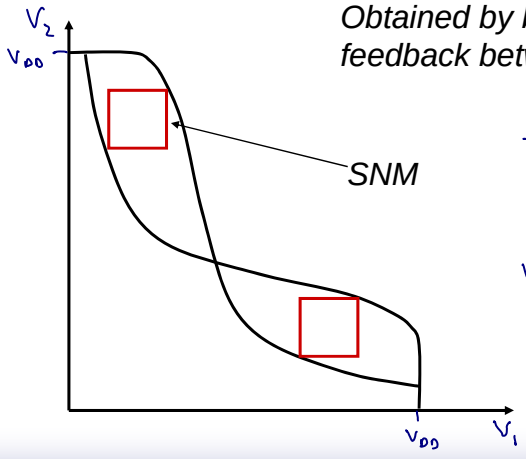
$$W_4 v_{sat} C_{ox} \frac{\left(V_{DD} - V_{Tp}\right)^2}{V_{DD} - V_{Tp} + \xi_{crit,p} L_4} = \mu_n C_{ox} \frac{W_6}{L_6}\left(V_{DD} - V_{Tn} - \frac{V_Q}{2}\right)V_Q$$

CMOS SRAM Analysis (Write)

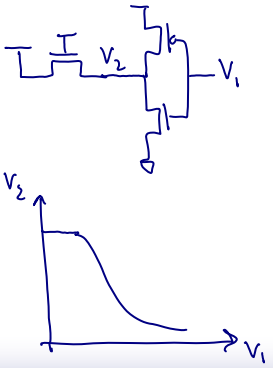


$$PR = \frac{(W/L)_4}{(W/L)_6}$$

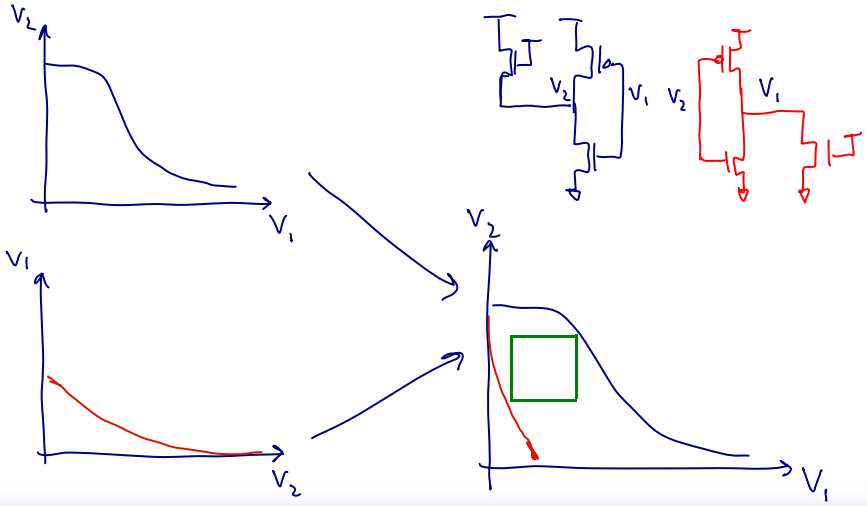
Read Static Noise Margin



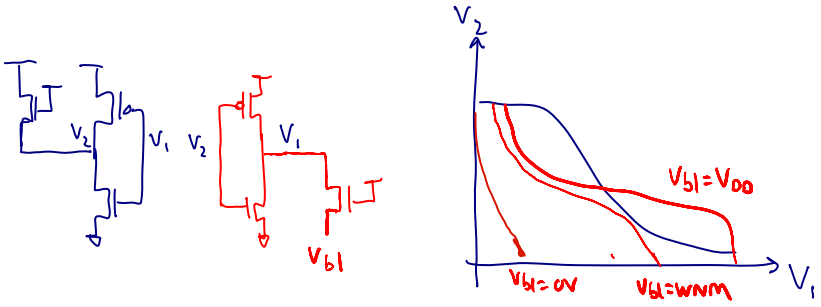
Obtained by breaking the feedback between the inverters



Write Static Noise Margin



Alternate Definition for Write Margin



WNM: max. V_{bl} where cell still flips

Next Lecture

- Power Revisited