Announcements

- Project #1 due Thursday

**Ratioed Logic**

Goal: build gates faster/smaller than static complementary CMOS

**Ratioed Logic**

- Spend power for speed
  - Use pseudo nMOS NOR gates, not NAND gates

- DC characteristics:
  - $V_{OH} = V_{DD}$
  - $V_{CL}$ depends on PMOS to NMOS ratio

**Pseudo-NMOS VTC**

<table>
<thead>
<tr>
<th>$W/L_p$</th>
<th>$V_{out}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
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<tr>
<td>2</td>
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<tr>
<td>4</td>
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<table>
<thead>
<tr>
<th>$V_{in}$ (V)</th>
<th>$V_{out}$ (V)</th>
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<tr>
<td>0.5</td>
<td>1.5</td>
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<td>1.5</td>
<td>0</td>
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</tbody>
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**Ratioed Logic LE**

- Rising and falling delays aren’t the same
  - Calculate LE for the two edges separately

- For $t_{pLH}$:
  - $C_{\text{gate}} = WC_G$
  - $C_{\text{inv}} = (3/2)WC_G$
  - $LE_{LH} = \ldots$

**Ratioed Logic Pull-down Delay**

- Think in terms of the current driving $C_{\text{load}}$

- When you have a conflict between currents
  - Available current is the difference between the two
  - In pseudo-nMOS case:
    \[ R_{\text{inv}} = \frac{1}{R_n + \frac{1}{R_p}} \rightarrow R_{\text{inv}} = \frac{R_n}{1 - \left(\frac{R_n}{R_p}\right)} \]
  - (Works because $R_p \gg R_n$ for good noise margin)

**Ratioed Logic LE (pull-down edge)**

- What is LE for $t_{pHL}$?
- Switch model would predict $R_{\text{off}} = R_n || R_p$
  - Would that give the right answer for LE?

**Response on Falling Edge**

- Time constant is smaller, but it takes more time to complete 50% $V_{DD}$ transient.
  - $R_p$ actually takes some current away from discharging $C$

**Improved Loads (2)**

- Differential Cascode Voltage Switch Logic (DCVSL)
**DCVSL Transient Response**

![DCVSL Transient Response graph]

**Pass-Transistor Logic**

- N transistors
- No static consumption

![Pass-Transistor Logic diagram]

**DCVSL Example 1**

**DCVSL AND:**

![DCVSL AND circuit diagram]

**Example: AND Gate**

\[ F = AB \]

![AND Gate circuit diagram]

**Pass-Transistor Logic**

**NMOS-Only Logic**

![NMOS-Only Logic circuit diagram]
NMOS-only Switch

Threshold voltage loss causes static power consumption.
NMOS has higher threshold than PMOS (body effect).

NMOS-Only Logic:
Level Restoring Transistor

Advantage:
- Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

Pass Transistor Logic LE

What is LE of “gate” shown below for A and B inputs?
- Hint: Can you answer this question with only the information shown below?

Restorer Sizing

Upper limit on restorer size:
- Pass-transistor pull-down can have several transistors in stack

Pass Transistor Logic LE

In CMOS, a “gate” is defined only when trace a connection all the way back to a supply:
- Otherwise don’t know what drive resistance really is
Restoring Full Swing: CPL

Resistance of Transmission Gate

CPL Level Restore

RC Model of Transmission Gate

Solution 2: Transmission Gate

Pass-Transistor Based Multiplexer
Next Lecture

- Dynamic Logic