EE141-Fall 2012 Digital Integrated Circuits

Lecture 19
Dynamic Logic

Announcements

- Midterm 2: Thurs. Nov. 1st, 6:30-8:00pm
  - Includes all material up to and including Lecture 18
  - Exam starts at 6:30pm sharp
  - Review session: Tues. evening?
- Project phase 2 out next Thurs., due following Fri.

Class Material

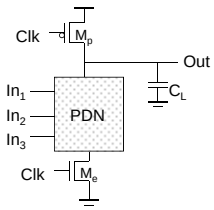
- Last lecture
  - Ratioed and Pass-Transistor Logic
- Today's lecture
  - Dynamic logic
- Reading
  - Chapter 6

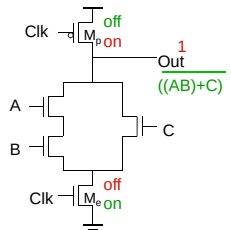
Dynamic Logic

Dynamic CMOS

- In static circuits, at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - only requires *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate



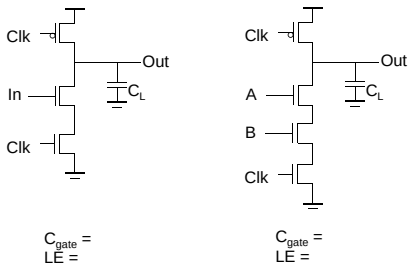


Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)

Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one rising transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

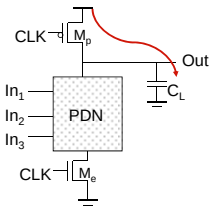
LE of Dynamic Gates



C_{gate} =
LE =

C_{gate} =
LE =

Power Consumption of Dynamic Gates



Power only dissipated when previous Out = 0

Dynamic Power Consumption is Data Dependent

Dynamic 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities
$P_{A=1} = 1/2$
$P_{B=1} = 1/2$

Then transition probability
$P_{0\to1} = P_{out=0} \times P_{out=1}$

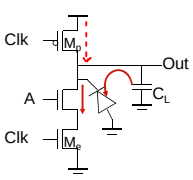
$= 3/4 \times 1 = 3/4$

Switching activity always higher in dynamic gates!
$P_{0\to1} = P_{out=0}$

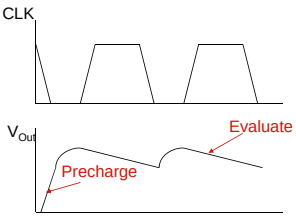
Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
- Needs a precharge/evaluate clock

Issues in Dynamic Design 1: Charge Leakage

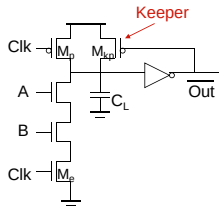


Leakage sources



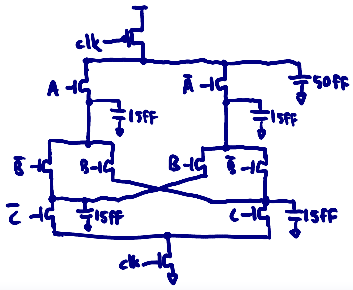
Dominant component is subthreshold current

Solution to Charge Leakage

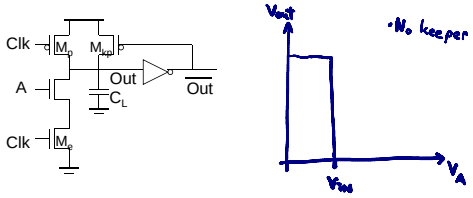


Same approach as level restorer for pass-transistor logic

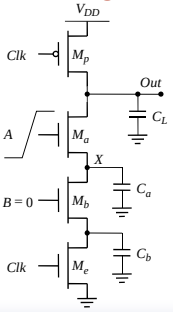
Charge Sharing Example



Dynamic Gate VTC



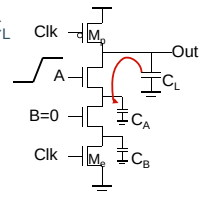
Charge Sharing



- Two cases:
  - M_a stays on – complete charge share
  - M_a turns off – incomplete charge share
- Complete charge share:
  - $Q_{Ca} = V_{Out}C_a$
    $\Delta Q_{CL} = -V_{Out}C_a$
  - → $\boxed{\Delta V_{Out} = -V_{DD}C_a/(C_a+C_L)}$
- Incomplete charge share:
  - $Q_{Ca} = (V_{DD}-V_{TN}^*)C_a$
    $\Delta Q_{CL} = -(V_{DD}-V_{TN}^*)C_a$
  - → $\boxed{\Delta V_{Out} = -(V_{DD}-V_{TN}^*)C_a/C_L}$

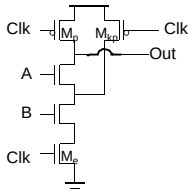
Issues in Dynamic Design 2: Charge Sharing

- Charge initially stored on C_L
  - C_A previously discharged



- When A rises, this charge is redistributed (shared) between C_L and C_A
- Makes Out drop below V_{DD}

Solution to Charge Sharing



- Keeper helps a lot
  - Can still get failures if Out drops below inverter V_{sw}
- Another option: precharge internal nodes
  - Increases power and area

Next Lecture

- Adders