Administrative Stuff

- Discussions start this Friday
- Labs start next week
- Homework #1 is due this Thursday
  - Everyone should have an EECS instructional account
  - Use cory, quasar, pulsar
HSPICE Syntax

Simple CMOS inverter

.include '/home/ff/ee141/MODELS/gpdk090_mos.sp' TT_s1v

* netlist
Vdd vdd 0 1.2
VIN in 0 PULSE 0 1.2 200ps 100ps 2ns 4ns
M0 out in vdd vdd gpdk090_pmos1V L=100e-9 W=120e-9
M1 out in gnd gnd gpdk090_nmos1V L=100e-9 W=120e-9
R1 in gnd 10K
R2 out vdd 100K

* extra control information
.options post=2 nomod

* analysis
.op
.TRAN .01ns 3ns
.DC VIN 0 1.2 .001
.END

Last Lecture

- Last lecture
  - Introduction, Moore’s law, future of ICs
- Today’s lecture
  - Introduce basics of integrated circuit manufacturing and cost
- Reading: Ch 2.1, 2.2
CMOS Manufacturing Process

The MOS Transistor

Polysilicon

Aluminum
**The Manufacturing Process**

For a complete walk-through of the process (64 steps), check the Book web-page

http://bwrc.eecs.berkeley.edu/IcBook

**Photo-Lithographic Process**

Typical operations in a single photolithographic cycle (from [Fullman]).
**Patterning of SiO₂**

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

(d) After development and etching of resist, chemical or plasma etch of SiO₂

(e) After etching

(f) Final result after removal of resist

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**Advanced Metallization**

Dual damascene IC process

- Oxide deposition
- Metal deposition
- Wire lithography and reactive ion etch
- Stud lithography and reactive ion etch
- Stud and wire metal deposition
- Metal chemical-mechanical polish

Source: IBM Corp.
A “Modern” CMOS Process

Dual-Well Shallow-Trench-Isolated CMOS Process

Transistor Layout
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.

- Recurrent costs - variable
  - Proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these related to chip area
NRE Cost is Increasing

Total Cost

- Cost per IC

\[
\text{cost per IC} = \frac{\text{variable cost per IC} \times \text{volume}}{\text{fixed cost}}
\]

- Variable cost

\[
\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}
\]
**Die Cost**

\[
\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}
\]

From: http://www.amd.com

**Wafer size**

- AMD Athlon
  - 8” (200mm) 90nm CMOS
  - 12” (300mm) 90nm CMOS
  - 12” (300mm) 65nm CMOS

From: http://www.sandpile.org
**Yield**

\[
Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%
\]

\[
\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}
\]

\[
\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}
\]

**Defects**

\[
\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}, \text{ where } \alpha \text{ is approximately 3}
\]

\[
\text{die cost} \propto \frac{1}{\left(\frac{\text{die/wafer} \times \text{die area}^{-1}}{\text{yield} \times \text{die area}^{-1}}\right)^\alpha} \times \text{die area}^4
\]
Cost per Transistor

Fabrication cost per transistor

cost: ¢-per-transistor

Next Lecture

- CMOS transistors as switches
- How to build an inverter
- Design metrics