EE141-Fall 2012 Digital Integrated Circuits

Lecture 2
Integrated Circuit Basics: Manufacturing and Cost

Administrative Stuff
- Discussions start this Friday
- Labs start next week
- Homework #1 is due this Thursday
  - Everyone should have an EECS instructional account
  - Use cory, quasar, pulsar

HSPICE Syntax
Simple CMOS inverter

```
.include '/home/ff/ee141/MODELS/gpdk090_mos.sp' TT_s1v

* netlist
Vdd vdd 0 1.2
VIN in 0 PULSE 0 1.2 200ps 100ps 2ns 4ns
M0 out in vdd gpdk090_mpos1V W=100e-9 L=100e-9
M1 out in gnd gpdk090_nmpos1V W=100e-9 L=100e-9
R1 in gnd 10K
R2 out vdd 100K
* extra control information
.options post=2 nomod
* analysis
.abc
.TRAN 0.01ns 3ns
.DC VIN 0 1.2 .001
.END
```

CMOS Manufacturing Process

The MOS Transistor

Polyisilicon

Last Lecture
- Last lecture
  - Introduction, Moore’s law, future of ICs
- Today’s lecture
  - Introduce basics of integrated circuit manufacturing and cost
- Reading: Ch 2.1, 2.2
The Manufacturing Process

For a complete walk-through of the process (64 steps), check the Book web-page
http://bwrc.eecs.berkeley.edu/icBook

Photo-Lithographic Process

Typical operations in a single photolithographic cycle (from [Fullman]).

Advanced Metallization

A “Modern” CMOS Process

Transistor Layout

Patterning of SiO₂
**Cost of Integrated Circuits**

- **NRE (non-recurrent engineering) costs - fixed**
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.

- **Recurrent costs - variable**
  - Proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these related to chip area

**Total Cost**

- **Cost per IC**
  \[
  \text{cost per IC} = \frac{\text{variable cost per IC}}{\text{volume}} + \text{fixed cost}
  \]

- **Variable cost**
  \[
  \text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}
  \]

**Die Cost**

- **Die cost**
  \[
  \text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}
  \]

**NRE Cost is Increasing**

**Wafer size**

- 8" (200mm)
- 12" (300mm)
- 12" (300mm)
- 65nm CMOS

From: http://www.sandpile.org
**Yield**

\[ \text{Yield} = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\% \]

\[ \text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}} \]

\[ \text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\sqrt{2} \times \text{die area}} \]

**Defects**

\[ \text{die yield} = \left( 1 + \alpha \frac{\text{defects per unit area} \times \text{die area}}{\text{die area}} \right)^{-\alpha}, \text{ where } \alpha \text{ is approximately 3} \]

\[ \text{die cost} \propto \left( \frac{\text{die wafer} \times \text{die area}^{-1} \times \text{yield}^{-1} \times \text{die area}^{-1}}{\text{die area}^{-1}} \right) \propto \text{die area}^{3} \]

**Cost per Transistor**

Fabrication cost per transistor