

*EE141-Fall 2012
Digital Integrated
Circuits*

Lecture 21
Multipliers

Announcements

- Project phase 2 out today, due next Fri.

- No lecture next Thurs. (11-8)

Class Material

- Last lecture
 - Adders
- Today's lecture
 - Multipliers

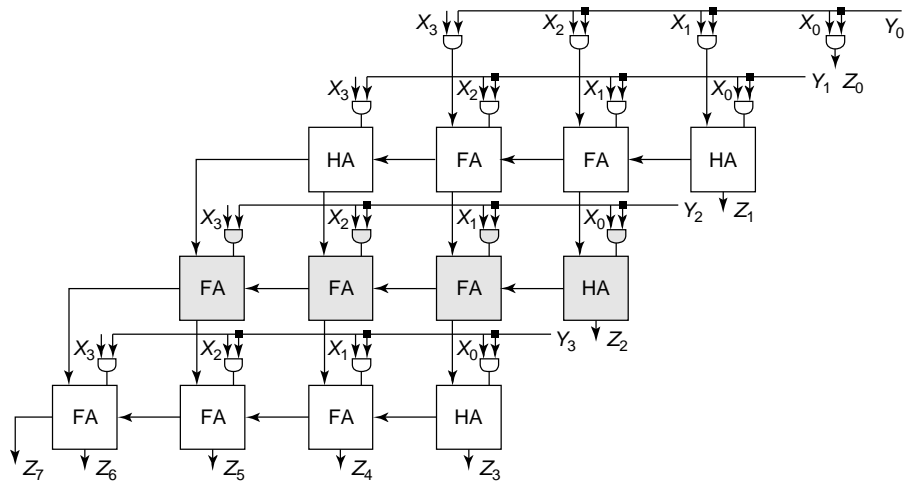


Multipliers

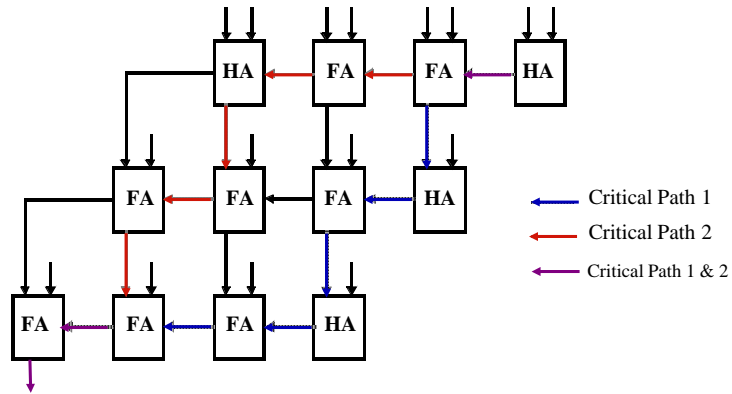
Binary Multiplication

	1 0 1 0 1 0	Multiplicand
x	1 0 1 1	Multiplier
	1 0 1 0 1 0	}
	1 0 1 0 1 0	
	0 0 0 0 0 0	
+	1 0 1 0 1 0	
	1 1 1 0 0 1 1 1 0	Result

The Array Multiplier

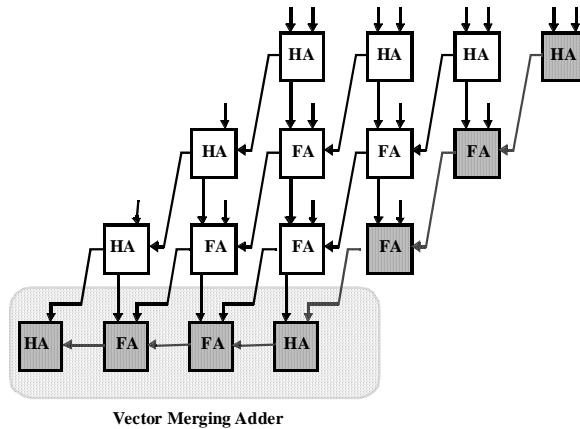


The M-by-N Array Multiplier: Critical Path



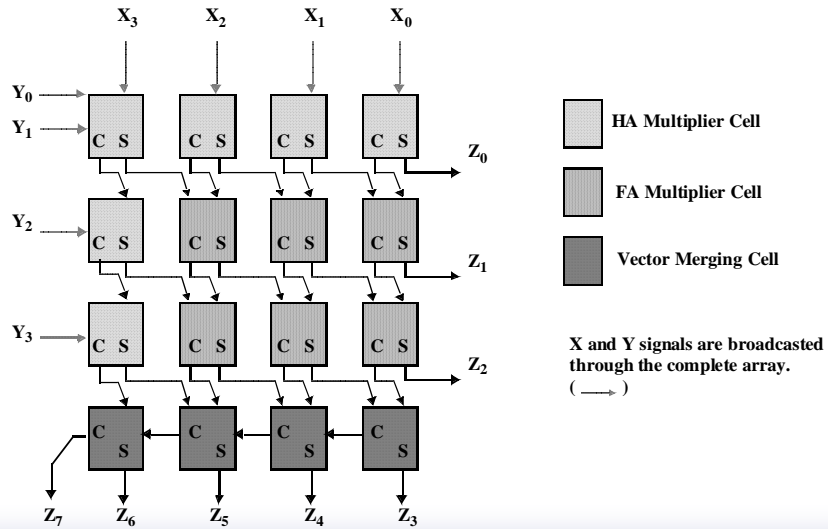
$$t_{mult} \approx [(M-1) + (N-2)] \cdot t_{carry} + (N-1) \cdot t_{sum} + t_{and}$$

Carry-Save Multiplier



$$t_{mult} = t_{and} + (N-1) \cdot t_{carry} + t_{merge}$$

Multiplier Floorplan

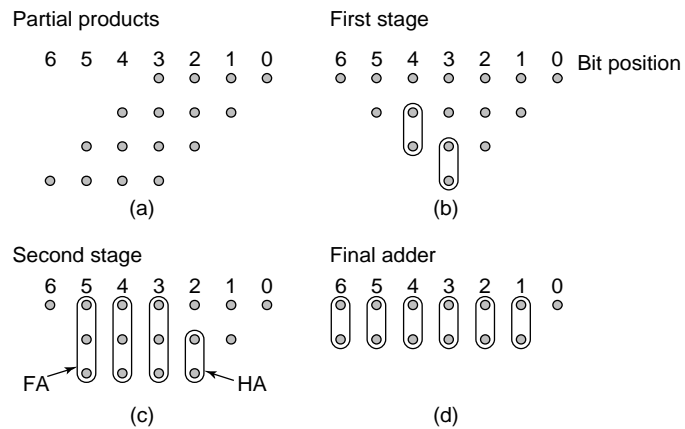


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Wallace-Tree Multiplier

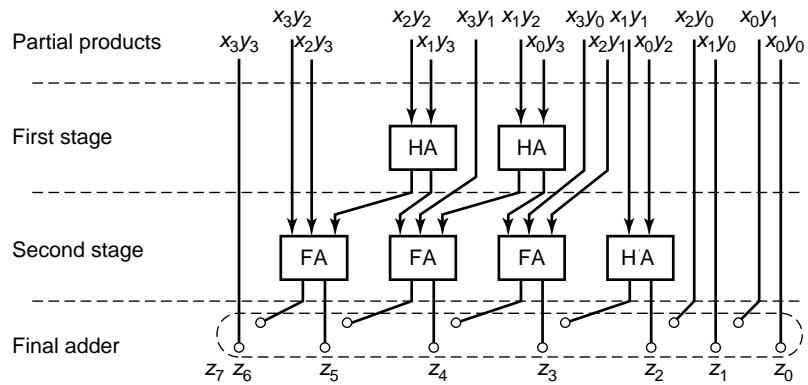


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Wallace-Tree Multiplier



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Multipliers – Summary

- Optimization constraints different than in binary adder
 - Once again:
 - Need to identify critical path
 - And find ways to use parallelism to reduce it
- Other possible techniques
 - Logarithmic versus linear (Wallace Tree Mult)
 - Data encoding (Booth)
 - Pipelining

First glimpse at system level optimization

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