




*EE141-Fall 2012
Digital Integrated
Circuits*

Lecture 21
Multipliers

EECS141 Lecture #21 1



Multipliers

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Announcements

- Project phase 2 out today, due next Fri.
- No lecture next Thurs. (11-8)

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Binary Multiplication

	1 0 1 0 1 0	Multiplicand
x	1 0 1 1	Multiplier
	1 0 1 0 1 0	} Partial products
	1 0 1 0 1 0	
	0 0 0 0 0 0	
+	1 0 1 0 1 0	} Result
	1 1 1 0 0 1 1 1 0	

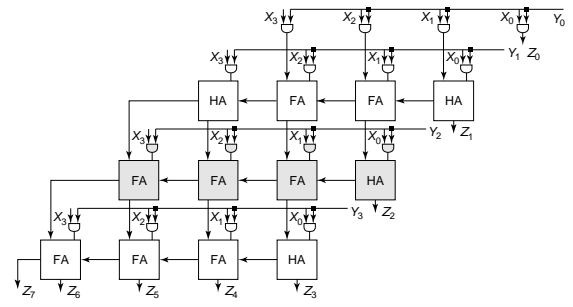
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Class Material

- Last lecture
 - Adders
- Today's lecture
 - Multipliers

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The Array Multiplier



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The M-by-N Array Multiplier: Critical Path

← Critical Path 1
← Critical Path 2
← Critical Path 1 & 2

$$t_{mult} \approx [(M-1) + (N-2)] \cdot t_{carry} + (N-1) \cdot t_{sum} + t_{and}$$

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Wallace-Tree Multiplier

Partial products: 6 5 4 3 2 1 0
 First stage: 6 5 4 3 2 1 0 Bit position
 Second stage: 6 5 4 3 2 1 0
 Final adder: 6 5 4 3 2 1 0

(a) (b) (c) (d)

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Carry-Save Multiplier

Vector Merging Adder

$$t_{mult} = t_{and} + (N-1) \cdot t_{carry} + t_{merge}$$

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Wallace-Tree Multiplier

Partial products: $x_3y_3, x_3y_2, x_2y_3, x_3y_1, x_1y_3, x_0y_3, x_2y_1, x_1y_2, x_3y_0, x_1y_1, x_0y_2, x_1y_0, x_0y_1$
 First stage
 Second stage
 Final adder: $z_7, z_6, z_5, z_4, z_3, z_2, z_1, z_0$

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Multiplier Floorplan

HA Multiplier Cell
 FA Multiplier Cell
 Vector Merging Cell

X and Y signals are broadcasted through the complete array. (→)

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Multipliers - Summary

- Optimization constraints different than in binary adder
 - Once again:
 - Need to identify critical path
 - And find ways to use parallelism to reduce it
- Other possible techniques
 - Logarithmic versus linear (Wallace Tree Mult)
 - Data encoding (Booth)
 - Pipelining

First glimpse at system level optimization

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