Announcements

- Project phase 2 due Friday
  - Phase 3 out this Friday

- Homework #8 out next Tues., due following Tues.
Class Material

- Last lecture
  - Multipliers
- Today’s lecture
  - Domino logic
- Reading
  - Chapter 7
Domino Logic

Why Named Domino?

Like falling dominos!
Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

Domino Logic LE

\[
\begin{align*}
LE_A &= 1 \\
LE_B &= 1 \\
\overline{LE} &= 1 \\
\overline{\overline{LE}} &= 1 \\
LE_{A\overline{A}} &= \frac{7}{3}
\end{align*}
\]
**Domino Logic LE (skewed static gate)**

Reference inverter:

\[
\text{LE}_{\text{inv}} = \frac{2}{3}
\]

**Buffer “Average” LE**

\[
\text{LE}_{\text{dinv}} = \frac{5}{6}
\]

\[
\text{TI} \text{LE} = \frac{10}{18} \approx \frac{5}{9}
\]

\[
\text{“Average” LE} = \sqrt{\text{TI} \text{LE}} \approx \frac{3}{4}
\]
Optimal EF/stage with Domino

- Domino buffers are faster than static CMOS inverters
- Is optimal EF/stage for a chain of domino gates still 4?

Example
**Designing with Domino Logic**

- **Inputs = 0 during precharge**
- **Can be eliminated**

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**Footless Domino**

- The first gate in the chain needs a foot switch
- Precharge is rippling – short-circuit current
**Footless Domino**

Can mitigate short-circuit current by alternating between footed and unfooted domino

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**Footless Domino**

To eliminate the short-circuit current, can delay the clock for each stage
**Differential (Dual Rail) Domino**

\[ \text{Out} = \overline{AB} \]

Allows inverting gates to be built

**np-CMOS**

Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN
NORA Logic

Fast, but EXTREMELY sensitive to noise!

Next Lecture

- Flops and Latches