EE141-Fall 2012 Digital Integrated Circuits

Lecture 22
Domino Logic

Announcements

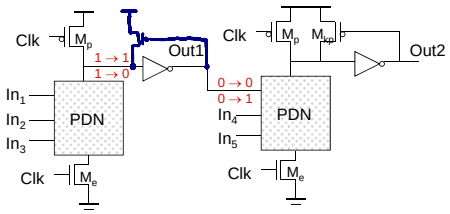
- Project phase 2 due Friday
  - Phase 3 out this Friday
- Homework #8 out next Tues., due following Tues.

Class Material

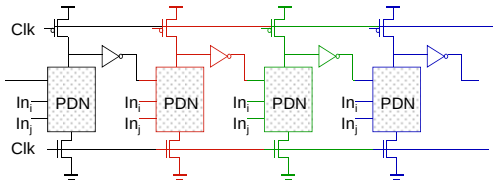
- Last lecture
  - Multipliers
- Today's lecture
  - Domino logic
- Reading
  - Chapter 7

Domino Logic

Domino Logic



Why Named Domino?

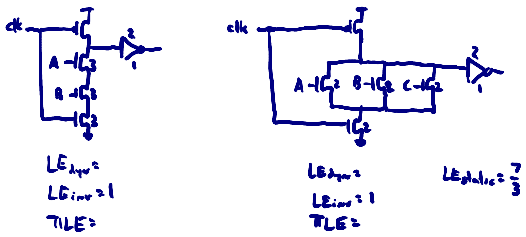


Like falling dominos!

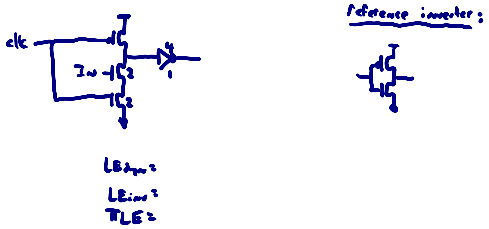
Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

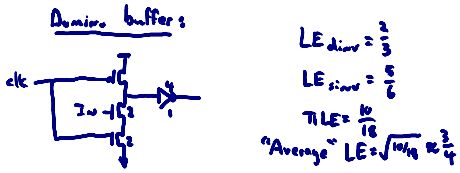
Domino Logic LE



Domino Logic LE (skewed static gate)



Buffer "Average" LE

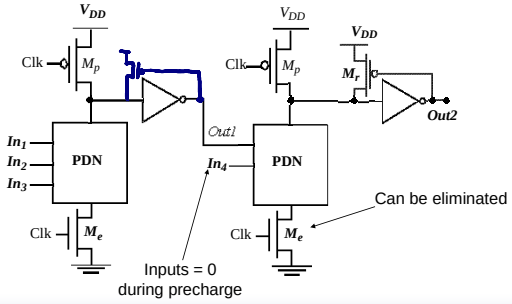


Optimal EF/stage with Domino

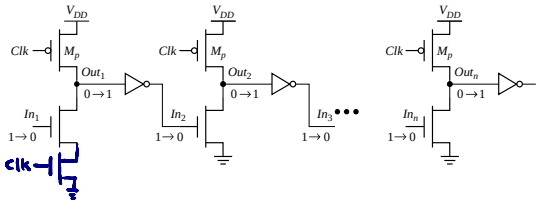
- Domino buffers are faster than static CMOS inverters
- Is optimal EF/stage for a chain of domino gates still 4?

Example

Designing with Domino Logic

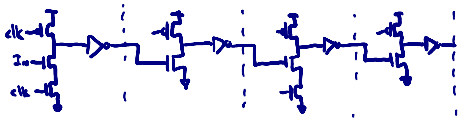


Footless Domino



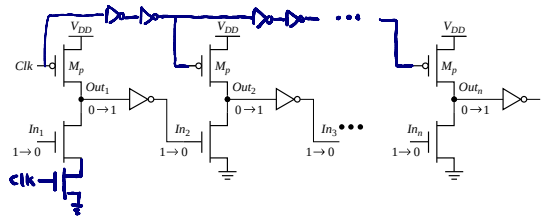
The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current

Footless Domino



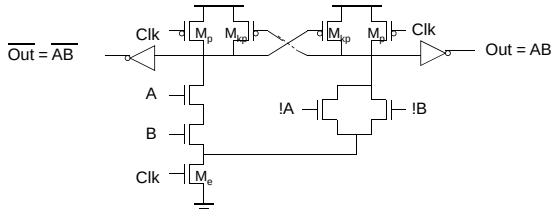
Can mitigate short-circuit current by alternating between footed and unfooted domino

Footless Domino



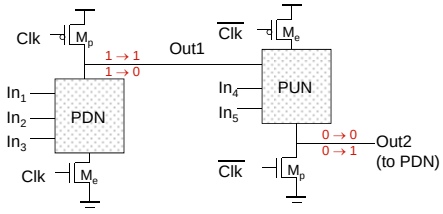
To eliminate the short-circuit current, can delay the clock for each stage

Differential (Dual Rail) Domino



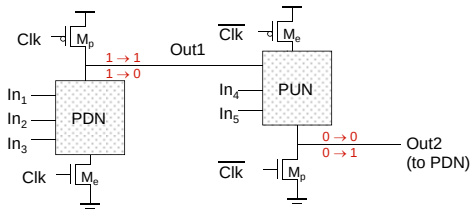
Allows inverting gates to be built

np-CMOS



Only $0 \rightarrow 1$ transitions allowed at inputs of PDN
Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

NORA Logic



Fast, but EXTREMELY sensitive to noise!

Next Lecture

- Flops and Latches